iPORT NTx-Deca User Guide

Pleora
Technologies

Table of Contents

Document Number and Revisions

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Revision	Reason for Revision	Date
3.0	Revision	October 2025
2.0	Several modification to tables, images and red track edit line removed.	May 2024
1.0	Initial Release	January 2024

1 About this Guide

This chapter describes the purpose and scope of this guide, and provides a list of complementary guides.

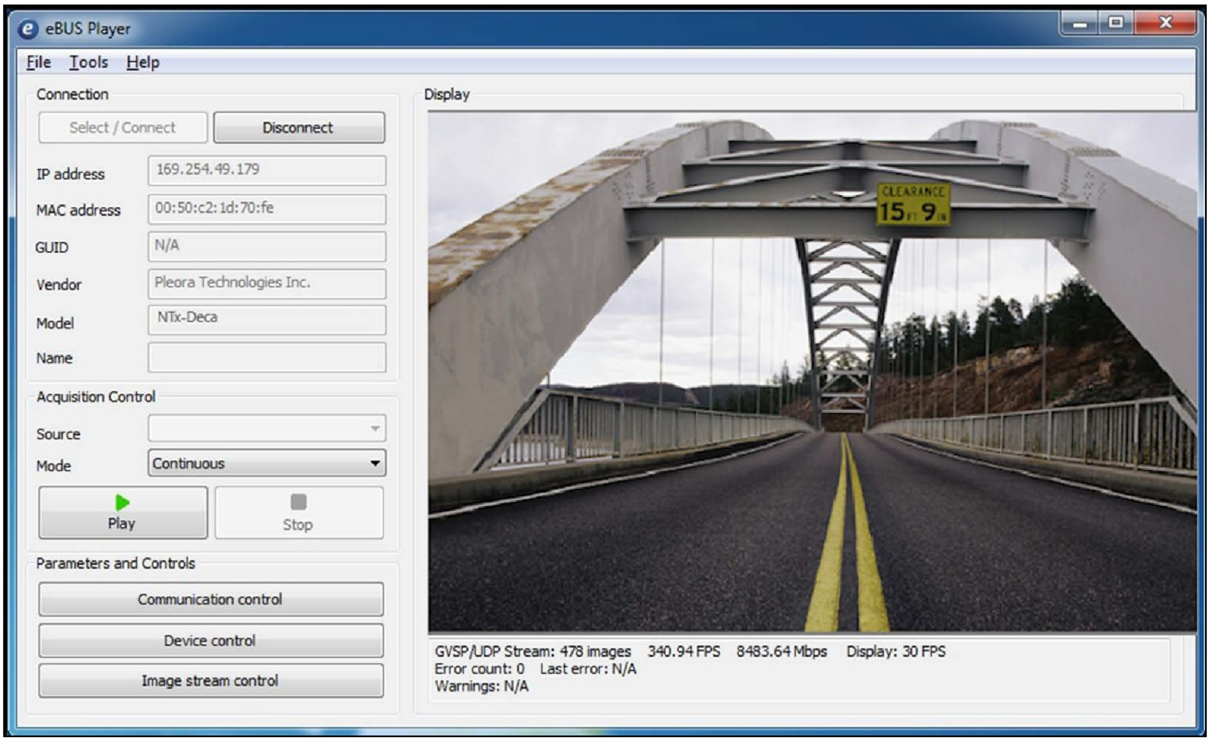
1.1 What this Guide Provides

This guide provides you with all of the information you need to connect the iPORT NTx-Deca to your sensor and related electronics to create a camera or other imaging device. In this guide you will find a product overview, connector details, and mechanical drawings, along with instructions for installing the Pleora eBUS™ SDK, connecting the device, and performing general configuration tasks to properly display video.
The last chapter of this guide provides Technical Support contact information for Pleora Technologies.

1.2 Start Streaming Video

If you want to quickly start streaming video, go to:

- "Confirming Image Streaming"
- "Configuring the NTx-Deca Image Settings"



1.3 Related Documents

The *iPORT NTx-Deca User Guide* is complemented by the following Pleora Technologies documents, which are available on the Pleora Technologies Support Center (https://supportcenter.pleora.com/):

- *eBUS Player Quick Start Guide* and *eBUS Player User Guide,* available for Windows, Linux, and macOS
- eBUS SDK AP Quick Start Guides, available for C++, .NET, Python and Linux
- *eBUS SDK API Help Files*
- *10G GigE Vision System Configuration Application Note*

The following guide is available from your Pleora Support representative, for customers who have purchased the Pleora AutoGen XML generation tool and Firmware Reference Design:

- *GenICam Integration Guide for Altera-Based Products*

1.4 Further Reading

Although not required in order to successfully use the embedded video interface, you can find details about industry-related standards and naming conventions in the following documents:

- *GigE Vision Standard, version 0* available from the Association for Advancing Automation (A3) Vision & Imaging at www.automate.org
- *GenICam Standard Features Naming Convention* available from the European Machine Vision Association (EMVA) at emva.org
- *Pixel Format Naming Convention, available from the EMVA at* emva.org
- *Camera Link Standard Specification*, available from the Association for Advancing Automation (A3) Vision & Imaging at automate.org

2 Dissipating Static Electricity

Electrostatic Discharge (ESD) is the sudden discharge of electricity between two charged objects. ESD damage to electronic components occurs when there is a difference in charge between objects. ESD damage can be prevented by equalizing the charge so that the electronic part, the work surface, and the person handling the part are all at the same charge.

The level of static electricity increases on your body and your clothing when you move around or come into contact with other charged surfaces. Excessive levels of static electricity can damage equipment.

2.1 ESD Protection and Handling Electrostatic Discharge Sensitive (ESDS) Products

You must wear a properly functioning and grounded wrist strap and ESD apparel (for example, an ESD smock) when handling Electrostatic Discharge Sensitive Devices (ESDS). You must also ensure that you handle or work on ESDS devices, such as printed circuit boards, on ESD-safe work surfaces.

 Do not use an ESD shielding bag as a work surface. ESD shielding bags may have surface resistance values that are higher than the required resistance to the ground. Set aside or discard the ESD bag after unpacking the device.

Wear wrist straps in close contact with a moist part of your skin. Connect the wrist strap's grounding cord to the common ground on a grounded workstation. You can also use heel grounders or similar worn footwear attachments if the floor is designed to dissipate static electricity. If the properties of the floor are unknown, use a wrist strap.

When unpacking ESDS parts, ensure that you are grounded and wearing ESD apparel before removing the part from its ESD shielding bag or container. ESDS products must be transported in ESD shielded bags, trays, containers, or carts. Ensure that conductive materials remain at least 30 cm (12 in.) away from ESDS products.

2.1.1 ESD Awareness Symbols

ESD awareness labels are based on the ANSI ESD Standards. Pleora products and documentation use the following symbols.

2.1.2 ESD Susceptibility Symbol

The ESD susceptibility symbol is used to identify devices and assemblies that are susceptible to ESD. Products with this label are static-sensitive and you must use ESD precautions when handling them.

2.1.3 ESD Protective Symbol

The ESD protective symbol, also known as the ESD packaging symbol, is used on packaging labels for products that have at least one ESD control property. The label may also include a letter to identify the product's most important ESD control property, as follows:

- L = Low Charging
- D = Static Dissipative
- C = Conductive EPA (for use in the ESD Protected Area)

2.1.4 ESD Common Point Ground Symbol

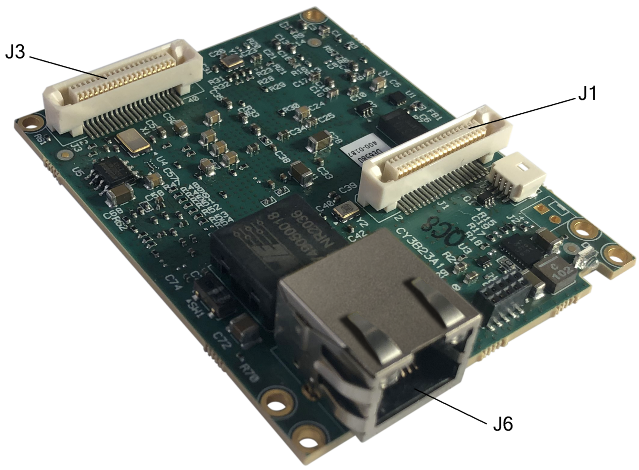
The ESD common point ground identifies a ground where two or more conductors are bonded, as defined by ANSI/ESD-S6.1. This label identifies the ground point for an ESD workstation.

2.2 About the iPORT NTx-Deca

This chapter describes the iPORT NTx-Deca, including the product models and key features.

Pleora's iPORT NTx-Deca hardware helps manufacturers shorten time-to-market, reduce risk, and lower costs by providing a straightforward way to integrate high-bandwidth GigE Vision® 2.0 video connectivity over 10GBASE-T into imaging devices and systems.

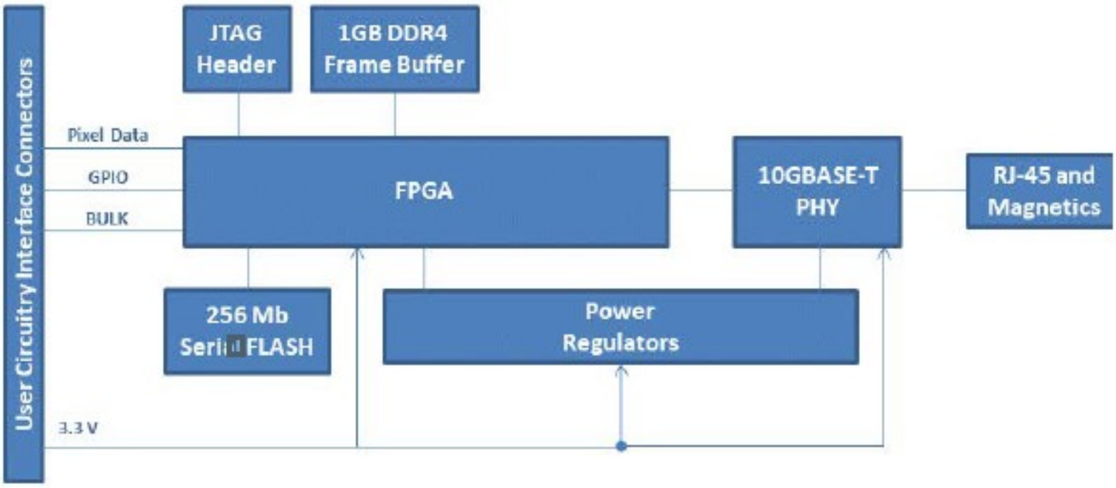
The NTx-Deca Embedded Video Interface is a compact transmitter that enables rapid and low-risk creation of GigE Vision 2.0-compliant cameras and other imaging devices. It enables the transmission of uncompressed high-bandwidth images at speeds of up to 10 Gbps over Cat6A cabling. The video interface complies with the GigE Vision 2.0 and GenICam™ standards, ensuring interoperability in multi-vendor networked or point-to-point digital video systems. The product supports the IEEE 1588 Precision Time Protocol to synchronize image capture functions and other system elements, enabling the exact triggering of image acquisition. Integrated image management allows you to track and retrieve images that are transmitted during a particular acquisition session.



Pleora's NTx-Deca is supported by:

- eBUS SDK, a feature-rich application development toolkit for manufacturers to rebrand and distribute with their end-products;
- The AutoGen XML generation tool and a firmware reference design, which make it fast and easy for manufacturers to create a user-friendly GenICam interface for their products.

Figure 1: NTx-Deca Block Diagram



2.3 NTx-Deca Models

The NTx-Deca is available in two models and is equipped with the parts listed in the following table.

Table 1: iPORT NTx-Deca Models

Order code	Model	Quantity
900-8025	iPORT NTx-Deca OEM Board	
	NTx-Deca OEM board with horizontal RJ-45 jack	1

Order code	Model	Quantity
900-8027	iPORT NTx-Deca Development Kit	
	NTx-Deca OEM board with horizontal RJ-45 jack mounted to a thermal baseplate	1
	10GBASE-T Ethernet desktop NIC	1
	Cat6a Ethernet cable (2 m)	1
	Power supply	1
	eBUS SDK USB stick	1

⚠ The NTx-Deca is designed to be used with a thermal solution or heat sink; otherwise, it will malfunction and can be damaged.

2.4 Feature Set

This section provides information about the iPORT NTx-Deca features.

Table 2: NTx-Deca General Features

General features

Number of channels	1
Scan modes	Area Scan (Progressive) and Line Scan
Pixel depth (bits)	8, 10, 12, 14, 16, 24, 30, 32, and 36 bits
Serial LVDS clock	37.5 MHz to 150 MHz
Taps per data channel	Up to 10 for internal 128-bit pixel depth parallel video bus
Image width (pixels)	• Minimum: 4 • Default: 640 • Maximum: 32 760 • The image width increment depends on the selected pixel format, taps per data and chunk mode selection.
Image height (pixels)	• Minimum: 1 • Default: 480 • Maximum: 32 767 • Increment: 1
Windowing/region of interest	Yes
Tap geometry	1X_1Y, 1X, 1X2_1Y, 1X2, 1X4_1Y, 1X4, 1X8_1Y, 1X8, 1X10_1Y, 1X10, 2X2E, 1XTR_2Y *, 1XTR_2YTR * * Tap geometries 1XTR_2Y and 1XTR_2YTR are non-standard and are not listed in the GenICam Standard Features Naming Convention. See “Supported Non-Standard Tap Geometries” on page 14 for more information.

Table 3: NTx-Deca Inputs/Outputs on the User Circuitry Interface

Inputs/outputs on user circuitry interface	
Video input	Serialized LVDS†
GPIO inputs	4 x 2.5 V LVCMOS**
GPIO outputs	3 x 2.5 V LVCMOS**

Serial (bulk)*	2 x 2.5 V LVCMOS**
Camera control outputs	4 x 2.5 V LVCMOS**

† For detailed signal specifications, see the characteristics of the sensor interface that are provided in "Sensor Interface" on page 45.

* The bulk interface ports support the UART (Universal Asynchronous Receiver/Transmitter), USRT (Universal Synchronous Receiver/Transmitter), I2C (Inter-Integrated Circuit), Serial Peripheral Interface (SPI), and High-Speed Download (HSD) protocols. For information about which protocols are supported on each bulk interface, see "Bulk Interfaces and Supported Protocols".

** For detailed signal specifications, see the characteristics of the inputs and outputs on the user circuitry connector that are provided in "40-Pin User Circuitry Interface Connector Pinouts".

Table 4: NTx-Deca Hardware

Hardware	
User circuitry interface (including power interface)	Two 40-pin Hirose connectors: FX6-40S-08SV2(93)
Network interface	RJ-45
10GBASE-T PHY	Marvell AQR113
Image buffer	1024 MB DDR4
Persistent memory	512 Mb Serial FLASH

Table 5: NTx-Deca Physical Characteristics

Physical characteristics	
Size (L x W x D)	72.5 mm x 56.0 mm x 17.6 mm (including RJ-45 jack)
Weight	32.5 grams
IC operating temperature range	Commercial[a]
Storage temperature	-40°C to 85°C
Operational humidity	Relative humidity of 30% to 75% (no condensation) at ambient temperature of 15°C to 30°C

Storage humidity	Relative humidity of 30% to 85% (no condensation) at ambient temperature of -10°C to 55°C
Power supply	3.3V +/- 5% (3.135 V to 3.465 V)
Typical power consumption, 30m CAT 6A cable, 9.2 Gbps	< 7 W
MTBF at 40° C	2,032,074 hours

[a] Using commercial temperature grade components. Case and junction temperature limits vary by IC device. See "Ambient and Junction Temperatures".

2.4.1 ESD Protection for High-Speed Data Lines

The NTx-Deca provides the following ultra-low capacitance ESD protection on Ethernet connections using a TVS array (SEMTECH, RCLAMP0522P.CT):

IEC 61000-4-2 (ESD) 17kV (air), 12kV (contact) IEC 61000-4-5 (Lightning) 5A (8/20us)

IEC 610000-4-4 (EFT) 40A (5/50ns)

2.5 Supported Non-Standard Tap Geometries

The iPORT NTx-Deca supports the 1xTR_2Y and 1xTR_2YTR tap geometries which are non-standard and therefore not documented in the *GenICam Standard Features Naming Convention (SFNC)*. The tap geometries are available over GenICam.

For these tap geometries, two segmented taps are enabled using pixel reversal (indicated by TR).

The following tables provide descriptions for the tap geometry configurations and the values of the six geometrical properties for each tap.

Table 6: 1XTR_2Y Tap Geometry

Geometry Name	Tap	X start	X end	X step	Y start	Y end	Y step
1XTR_2Y	Tap0	W	2	-1	1	H/2	1
	Tap1	1	W-1	1	(H/2)+1	H	1

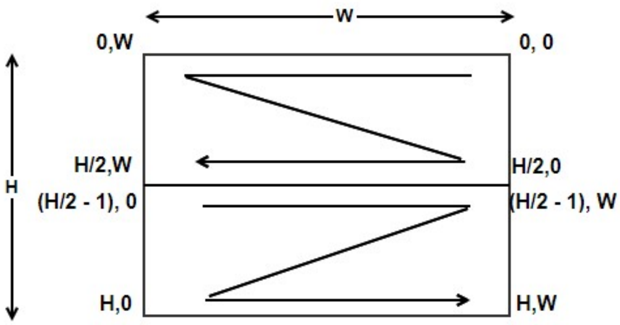
Table 7: 1XTR_2YTR Tap Geometry

Geometry Name	Tap	X start	X end	X step	Y start	Y end	Y step

1XTR_2YTR	Tap0	W	1	-1	H/2	1	-1
	Tap1	1	W	1	(H/2) +1	H	1

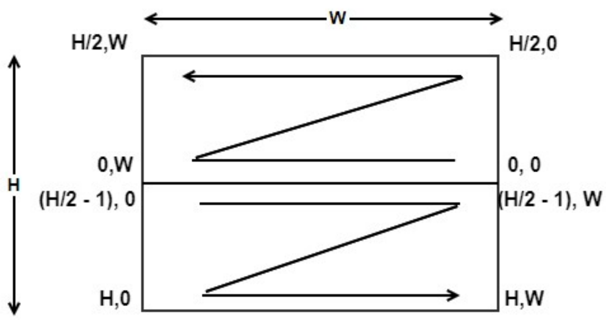
The following images illustrate the sensor readout formats for the tap geometries, as shown in the previous tables.

Figure 2: 1XTR_2Y Tap Geometry Sensor Readout



One zone in X with pixel reversal, two zones in Y.

Figure 3: 1XTR_2YTR Tap Geometry Sensor Readout



One zone in X with pixel reversal, two zones in Y with pixel reversal.

2.6 Selected GenICam Features

The NTx-Deca supports the seven features mandated by the GigE Vision standard along with additional features, some of which are listed in the following table. The full list of features can be seen in the Device Control dialog box of Pleora's eBUS Player application.

Table 8: Selected GenICam Features

Feature	Description

Width	Specifies the width of the image (in pixels).
Height	Specifies the height of the image (in pixels).
OffsetX	Specifies the horizontal image offset (in pixels).
OffsetY	Specifies the vertical image offset (in pixels).
PixelFormat	Specifies the format of the pixel provided by the device. Available pixel formats are: • Monochrome pixel formats, 8 to 32 bits • Bayer pixel formats, 8 to 16 bits • RGB and BGR, 24 to 36 bits • Sparse Color Filter pixel layouts, 8 to 12 bits • YUV pixel formats, 8 bits • YCbCr pixel formats, 8 bits
DeviceTapGeometry	Describes the geometrical properties characterizing the taps of a Camera Link camera, as seen from the frame grabber or acquisition card. This device tap geometry feature is defined in the GenICam SFNC. Available tap geometries are: • Geometry_1X_1Y • Geometry_1X2_1Y • Geometry_1X • Geometry_1X2 • Geometry_1X4_1Y • Geometry_1X4 • Geometry_2X2E • Geometry_1X8_1Y • Geometry_1X8 • Geometry_1X10_1Y • Geometry_1X10 • Geometry_1XTR_2Y * • Geometry_1XTR_2YTR *
DeviceScanType	Specifies the sensor scan type, such as Area Scan or Line Scan.
SensorDigitizationTaps	Specifies the number of digitized samples output simultaneously by the camera, 1, 2, 4, 8, or 10 taps.

* Geometries 1XTR_2Y and 1XTR_2YTR are non-standard and are not described in the *GenICamStandard Features Naming Convention (SFNC)*.

2.7 NTx-Deca Pixel Formats

The pixel formats available on the NTx-Deca are listed in the following table.

Table 9: NTx-Deca Pixel Formats

Taps	Pixel format			
1, 2, 4, 8, 10 taps	Mono8 (Default)	Mono8s		
1, 2, 4, 8 taps	Mono10	Mono10Packed	Mono10p	
1, 2, 4, 8 taps	Mono12	Mono12Packed	Mono12p	
1, 2, 4, 8 taps	Mono14			
1, 2, 4 taps	Mono14p			
1, 2, 4, 8 taps	Mono16			
1, 2, 4 taps	Mono32			
1, 2, 4, 8, 10 taps	BayerGR8	BayerRG8	BayerGB8	BayerBG8
1, 2, 4, 8 taps	BayerGR10	BayerRG10	BayerGB10	BayerBG10
1, 2, 4, 8 taps	BayerGR10p	BayerRG10p	BayerGB10p	BayerBG10p
1, 2, 4, 8 taps	BayerGR12	BayerRG12	BayerGB12	BayerBG12
1, 2, 4, 8 taps	BayerGR12p	BayerRG12p	BayerGB12p	BayerBG12p
1, 2, 4, 8 taps	BayerGR10Packed	BayerRG10Packed	BayerGB10Packed	BayerBG10Packed
1, 2, 4, 8 taps	BayerGR12Packed	BayerRG12Packed	BayerGB12Packed	BayerBG12Packed

1, 2, 4, 8 taps	BayerGR14	BayerRG14	BayerGB14	BayerBG14
1, 2, 4 taps	BayerGR14p	BayerRG14p	BayerGB14p	BayerBG14p
1, 2, 4, 8 taps	BayerGR16	BayerRG16	BayerGB16	BayerBG16
1, 2 taps	RGB8	BGR8		
1, 2 taps	RGBA8	BGRA8		
1, 2 taps	RGB10	BGR10		

Table 9: NTx-Deca Pixel Formats (Continued)

Taps	Pixel format			
1, 2 taps	RGB12	BGR12		
1, 2, 4, 8 taps	SCF1WGWR8	SCF1WGWR10	SCF1WGWR12	
1, 2, 4, 8 taps	YUV411_8_UYYVYY	YUV422_8_UYVY		
1, 2 taps	YUV8_UYV			
1, 2, 4, 8 taps	YCbCr601_422_8_ CbYCrY	YCbCr709_422_8_ CbYCrY		

3 NTx-Deca External Connections

This chapter describes the NTx-Deca external connections.

3.1 NTx-Deca Connector Locations

The following figure and table describe the NTx-Deca Embedded Video Interface connectors.

Figure 4: iPORT NTx-Deca Connectors.

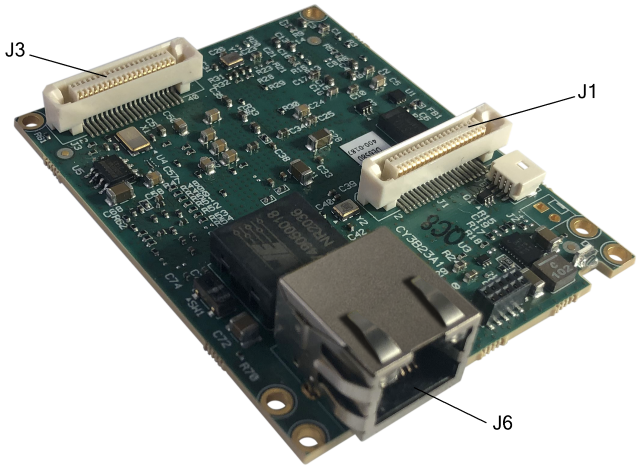
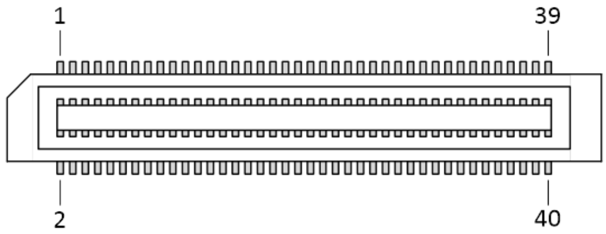


Table 10: NTx-Deca Connector Descriptions

ID	Type	Description
J1, J3	40-pin user circuitry interface	Interfaces directly to the imaging device, such as an X-ray flat panel detector or camera, and for powering at 3.3 volts +/-5% (3.135V-3.465), 2.42A (8W) maximum (100-meters Ethernet cable, 105C junction T of PHY, ~10Gbps streaming)
J6	RJ-45 Ethernet connector	Interfaces the NTx-Deca to Ethernet networks, as specified in IEEE 802.3. The Ethernet interface can operate at 1, 2.5, 5, and 10 Gbps, and supports Internet Protocol Version 4 (IPv4).

3.2 40-Pin User Circuitry Interface Connector Pinouts

The tables in this section provide the pinouts for the NTx-Deca 40-pin user circuitry connectors, J1 and J3.



The following table lists the characteristics for the single-ended I/Os on the user circuitry interface connectors (J1 and J3).

Table 11: 2.5 V LVCMOS and LVDS on the NTx-Deca

2.5 V LVCMOS I/Os	
VIL, minimum, absolute	-0.5 V
VIL, minimum	-0.3 V
VIL, maximum	0.7 V
VIH, minimum	1.7 V
VIH, maximum	2.8 V
VIH, maximum, absolute	3.8 V
VOL, minimum	0 V
VOL, maximum	0.4 V
VOH, minimum	2.1 V
VOH, maximum	2.625 V

LVDS-IN	
Absolute minimum	-0.5 V

Absolute maximum	3.8 V
VICM, minimum *	0.3 V
VICM, maximum *	1.425 V
VID, minimum **	0.1 V
VID maximum **	0.6 V
RD, minimum ***	65 Ohm
RD, nominal ***	100 Ohm
RD, maximum ***	135 Ohm
VIN, minimum	-0.3 V
VIN, maximum	2.1 V

* VICM — input common-mode voltage (DC coupling)

** VID — input differential voltage

*** RD — differential resistance (inside the FPGA)

The following table lists the pinouts of the J3 40-pin user circuitry interface connector.

Table 12: J3 User Circuitry Interface Connector Pinouts

Pin	Signal Name	Type	Direction	Description
1	GND	GND	—	Ground
2	GND	GND	—	Ground
3	LVDS0_CLK_P	LVDS	IN	Data clock positive polarity
4	LVDS0_DATA0_P	LVDS	IN	Data 0 positive polarity

5	LVDS0_CLK_N	LVDS	IN	Data clock negative polarity
6	LVDS0_DATA0_N	LVDS	IN	Data 0 negative polarity
7	GND	GND	—	Ground
8	GND	GND	—	Ground
9	LVDS0_DATA1_P	LVDS	IN	Data 1 positive polarity
10	LVDS0_DATA2_P	LVDS	IN	Data 2 positive polarity
11	LVDS0_DATA1_N	LVDS	IN	Data 1 negative polarity
12	LVDS0_DATA2_N	LVDS	IN	Data 2 negative polarity
13	+3.3V	PWR	—	Power input[a]
14	+3.3V	PWR	—	Power input[a]
15	LVDS0_DATA3_P	LVDS	IN	Data 3 positive polarity
16	LVDS0_DATA4_P	LVDS	IN	Data 4 positive polarity
17	LVDS0_DATA3_N	LVDS	IN	Data 3 negative polarity
18	LVDS0_DATA4_N	LVDS	IN	Data 4 negative polarity
19	BULK0_CS/CC1	2.5 V	OUT	Bulk interface 0 SPI chip select when SPI mode is selected. Bulk interface 0 HSD chip select when HSD mode is selected. Otherwise, connected to the PLC, signal Pb0CC0.

20	BULK0_RX	2.5 V	IN, OUT	Bulk interface 0 UART and USRT input, SPI MISO signal, and HSD SOUT1

Table 12: J3 User Circuitry Interface Connector Pinouts (Continued)

Pin	Signal Name	Type	Direction	Description
21	BULK0_TX	2.5 V	IN, OUT	Bulk interface 0 UART and USRT output, I2C input/open drain output, SPI MOSI signal, and HSD SOUT0
22	BULK0_CLK	2.5 V	IN, OUT	Bulk interface 0 USRT, I2C, SPI output clock, and HSD output clock
23	LVDS0_DATA5_P	LVDS	IN	Data 5 positive polarity
24	LVDS0_DATA6_P	LVDS	IN	Positive Polarity of serialized Frame (camera/sensor) synchronization signals: FVAL(bit0), LVAL (bit1), DVAL(bit2), and SPR(bit3).
25	LVDS0_DATA5_N	LVDS	IN	Data 5 negative polarity
26	LVDS0_DATA6_N	LVDS	IN	Negative Polarity of serialized Frame (camera/sensor) synchronization signals: FVAL(bit0), LVAL (bit1), DVAL(bit2), and SPR (bit3).
27	+3.3V	PWR	—	Power input[a]
28	+3.3V	PWR	—	Power input[a]
29	LVDS0_DATA7_P	LVDS	IN	Data 7 positive polarity
30	LVDS0_DATA8_P	LVDS	IN	Data 8 positive polarity
31	LVDS0_DATA7_N	LVDS	IN	Data 7 negative polarity

32	LVDS0_DATA8_N	LVDS	IN	Data 8 negative polarity
33	GND	GND	—	Ground
34	GND	GND	—	Ground
35	PB0_CTRL_OUT1	2.5 V	OUT	Connected to the PLC, signal Pb0CC1
36	GPIO_OUT2	2.5 V	OUT	GPIO OUT 2
37	PB0_CTRL_OUT2	2.5 V	OUT	Connected to the PLC, signal Pb0CC2
38	PWR_ON_RSTN	3.3 V	IN, OUT, OC	Power on Reset[b]
39	GND	GND	—	Ground
40	GND	GND	—	Ground

[a] 3 V input, 0.5 A maximum current rating per pin. Maximum current required at 3.3 V from the power regulator is 2.42 A (8.0W). There is no filter or protection for this pin.

[b] **PWR_ON_RSTN** is a bidirectional open collector pin with a 10 KOhm resistor to +3.3 V on the NTx-Deca This signal is high when power on the NTx-Deca is at the appropriate levels. You can do any of the following:

- Leave the pin set to C.
- Connect the signal to the open-collector/open-drain power ready signal of the user When you drive the signal low, it holds the embedded video interface in reset.
- Use the signal to start the configuration of user devices, such as FPGAs or
- Use the signal to initiate a reset of the embedded video interface A minimum low pulse width of 2 us is required.

The following table lists the pinouts of the J1 40-pin user circuitry interface connector.

Table 13: J1 User Circuitry Interface Connector Pinouts

Pin	Signal Name	Type	Direction	Description
1	GND	GND	—	Ground
2	GND	GND	—	Ground
3	LVDS0_DATA9_P	LVDS	IN	Data 9 positive polarity
4	LVDS0_DATA10_P	LVDS	IN	Data 10 positive polarity
5	LVDS0_DATA9_N	LVDS	IN	Data 9 negative polarity
6	LVDS0_DATA10_N	LVDS	IN	Data 10 negative polarity
7	GND	GND	—	Ground
8	GND	GND	—	Ground
9	LVDS0_DATA11_P	LVDS	IN	Data 11 positive polarity
10	LVDS0_DATA12_P	LVDS	IN	Data 12 positive polarity
11	LVDS0_DATA11_N	LVDS	IN	Data 11 negative polarity
12	LVDS0_DATA12_N	LVDS	IN	Data 12 negative polarity
13	+3.3V	PWR	—	Power input[a]

14	+3.3V	PWR	—	Power input[a]
15	LVDS0_DATA13_P	LVDS	IN	Data 13 positive polarity
16	LVDS0_DATA14_P	LVDS	IN	Data 14 positive polarity
17	LVDS0_DATA13_N	LVDS	IN	Data 13 negative polarity
18	LVDS0_DATA14_N	LVDS	IN	Data 14 negative polarity
19	BULK1_CLK	2.5V	IN, OUT	Bulk interface 1 USRT, I2C, and SPI clock
20	BULK1_RX	2.5V	IN, OUT	Bulk interface 1 UART and USRT input, and SPI MISO signal[b]

Table 13: J1 User Circuitry Interface Connector Pinouts (Continued)

Pin	Signal Name	Type	Direction	Description
21	BULK1_TX	2.5V	IN, OUT	Bulk interface 1 UART and USRT output, I2C input/open drain output, and SPI MOSI
22	FPGA_GPIO_IN2	2.5V	IN	Connected to the PLC, signal GpioIn2[b]
23	LVDS0_DATA15_P	LVDS	IN	Data 15 positive polarity
24	LVDS0_DATA16_P	LVDS	IN	Data 16 positive polarity
25	LVDS0_DATA15_N	LVDS	IN	Data 15 negative polarity
26	LVDS0_DATA16_N	LVDS	IN	Data 16 negative polarity

27	+3.3V	PWR	—	Power input[a]
28	+3.3V	PWR	—	Power input[a]
29	FPGA_GPIO_IN3	2.5 V	IN	Connected to the PLC, signal GpioIn3[b]
30	FPGA_GPIO_OUT1	2.5 V	OUT	Connected to the PLC, signal GpioOut1. Bulk interface 0 HSD SOUT3.
31	FPGA_GPIO_IN0	2.5 V	IN	Connected to the PLC, signal GpioIn0[b]
32	FPGA_GPIO_OUT0	2.5 V	OUT	Connected to the PLC, signal GpioOut0. Bulk interface 0 HSD SOUT2.
33	GND	GND	—	Ground
34	GND	GND	—	Ground
35	FPGA_GPIO_IN1	2.5 V	IN	Connected to the PLC, signal GpioIn1[b]
36	BULK1_CS/CC4	2.5 V	OUT	Connected to the PLC, signal Pb0CC3. Bulk interface 1 SPI chip select or Camera Control 4
37	Not used	DNC	—	Do Not Connect
38	Not used	DNC	—	Do Not Connect
39	GND	GND	—	Ground
40	GND	GND	—	Ground

[a]3 V input, 0.5 A maximum current rating per pin. Maximum current required at 3.3 V from the power regulator is 2.42 A (8.0 W). There is no filter or protection for this pin.

[b] If you do not use these pins, we recommend that you tie them to GND instead of leaving them unconnected.

3.3 Status LEDs

The NTx-Deca has status LEDs that indicate the operating status of the network connection, the power, and the firmware, as described in the following image and table.

Figure 5: NTx-Deca status LED locations

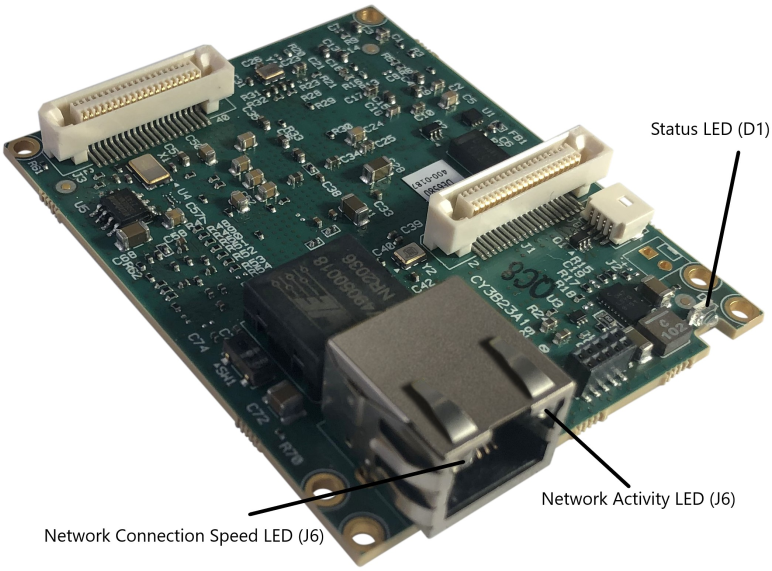


Table 14: NTx-Deca Status LED Descriptions

LED	ID	Description
Status	D1	Yellow and green off: Power is not supplied or no firmware load was programmed Yellow solid on: The backup firmware load is running Green solid on: The main firmware load is running
Network Connection Speed	J6	Off: 1 Gbps/1000BASE-T connection Yellow blinking: 0.77 Hz: 2.5 Gbps, 2.5GBASE-T connection Yellow blinking: 3.1 Hz, 5 Gbps, 5GBASE-T connection Yellow solid on: 10 Gbps, 10GBASE-T connection
Network Activity	J6	Green off: No Ethernet connection Green solid on: Ethernet link Green blinking: Data is being transmitted or received

4 Ambient and Junction Temperatures

This chapter provides you with the information you need to ensure the optimal operating temperature for your NTx-Deca.

⚠ The NTx-Deca is designed to be used with a thermal solution or heat sink; otherwise, it will malfunction and can be damaged.

4.1 Customer Requirements

The customer requirements are as follows:

- Customers are responsible for reading and understanding this entire ‘Ambient and Junction Temperatures’ chapter of this user
- Customers are responsible for obtaining and understanding additional thermal design information from the component manufacturers listed in Table
- Customers are responsible for implementing a thermal solution that maintains the Components listed in Table 15 at junction and case temperatures below the specified temperatures listed in Table 15 under the maximum thermal load and system conditions for their use
- Customers are responsible for qualification of the NTx-Deca in their system and are responsible for any issues related to failure to qualify the product

The following figures show the location of the PHY, FPGA, and DDR4 memory components. These components consume the largest amount of power on the NTx-Deca, and will therefore be most affected by high temperatures.

Figure 6: NTx-Deca bottom view

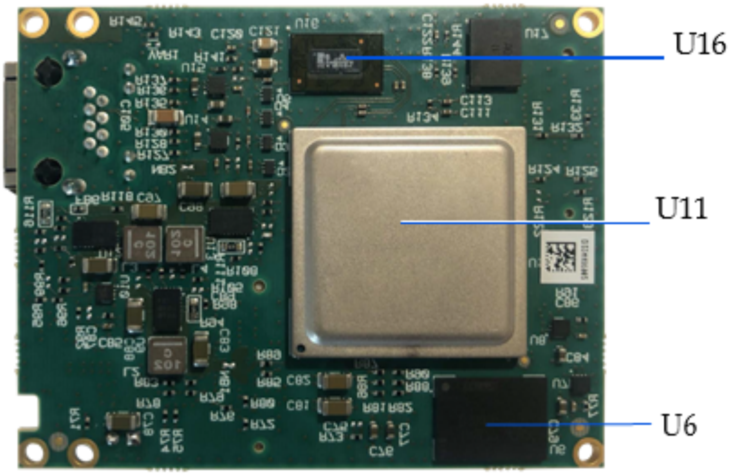
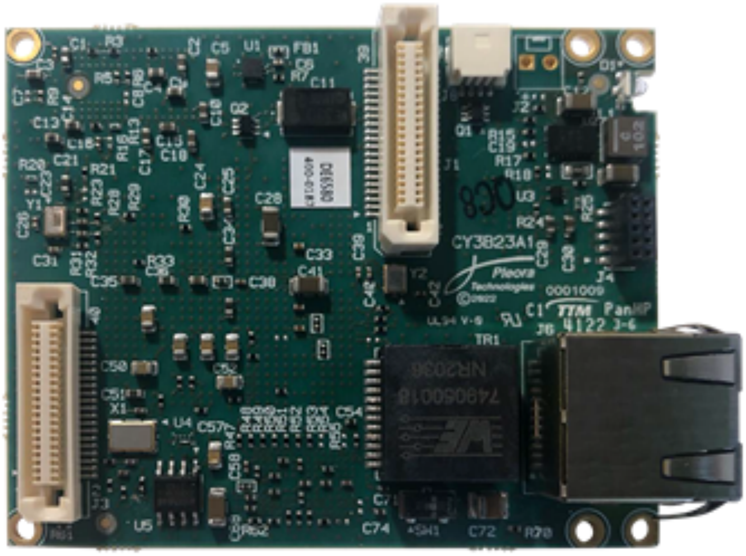


Figure 7: NTx-Deca top view



The following table outlines the components that consume the largest amount of power on the NTx-Deca and will therefore be most affected by high temperatures, and provides thermal guidelines, including ambient and junction temperatures.

Table 15: NTx-Deca Thermal Guidelines

Reference designator	Component and manufacturer part number	Manufacturer thermal specifications*
U11	FPGA Xilinx XCAU15P-1FFVB676E	TJ: 0°C to +100°C TC: Not specified ΘJC: 0.25°C/W ΘJB: 2.07°C/W ΘJA: 10.2°C/W ΘJA-Effective: 7.1°C/W at 250 LFM ΘJA-Effective: 6.0°C/W at 500 LFM ΘJA-Effective: 5.6°C/W at 750 LFM Power consumption: ~ 4500 mW**
U16	PHY Marvell AQR113-B1-C	TJ: 0°C to +108°C TC: Not specified ΘJC: 0.10°C/W ΘJB: 6.74°C/W ΘJA: 21.22°C/W Power consumption: ~1870 mW typical, ~ 2850 mW**
U6	DDR4 Micron MT40A512M16LY-062E:E	TJ: Not specified TC: 0°C to +85°C ΘJC(TOP): 4.8°C/W ΘJB: 15.2°C/W Power consumption: ~ 270 mW**

Important Notes:

* All thermal information is from the manufacturer’s documentation, and is for still air unless otherwise specified. All thermal resistance values are typical. For further details and thermal models, contact the component manufacturer.

** Using 100 m Cat 6A cable at 9.2 Gbps.

5 Bulk Interfaces

This chapter describes the bulk interfaces available on the NTx-Deca, and the supported protocols.

5.1 Bulk Interfaces and Supported Protocols

The NTx-Deca has two bulk interface ports available for serial communication, Bulk0 and Bulk1. Each bulk interface port supports the following:

- Standard UART (Universal Asynchronous Receiver/Transmitter)
- USRT (Universal Synchronous Receiver/Transmitter)
- I2C (Inter-Integrated Circuit) protocols, and Serial Peripheral Interface (SPI) protocol One bulk interface port (Bulk0) supports High-Speed Download protocol (HSD).

The bulk interface ports are available on the 40-pin user circuitry connectors, as outlined in the following table.

Table 16: NTx-Deca Bulk Interface and Connector Pinouts

Pin	Bulk signal name	Bulk mode				
		UART	USRT	I2C	SPI	HSD
J3 40-pin user circuitry connector						
19	BULK_CS0				SS	SS
20	BULK_RX0	RXD	RXD		MISO	SOUT1
21	BULK_TX0	TXD	TXD	SDA	MOSI	SOUT0
22	BULK_CLK0		SCK	SCL	SCLK	SCLK
J1 40-pin user circuitry connector						
19	BULK_CLK1		SCK	SCL	SCLK	
20	BULK_RX1	RXD	RXD		MISO	
21	BULK_TX1	TXD	TXD	SDA	MOSI	

30	FPGA_GPIO_OUT1					SOUT3 (Quad HSD only)*
32	FPGA_GPIO_OUT0					SOUT2 (Quad HSD only)*
36	BULK_CS1				SS	

* When QHSD is selected in the **BulkMode** list, these two FPGA_GPIO_OUT signals become Quad HSD SOUT signals.

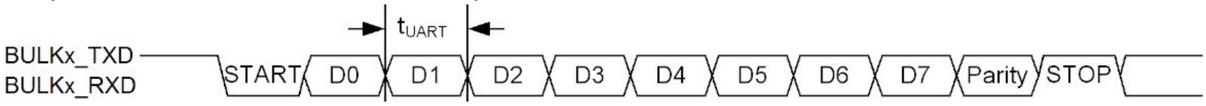
Tie unused pins to GND instead of leaving them disconnected.

The bulk interfaces on the NTx-Deca are 2.5 V LVCMOS. For detailed signal specifications, see the characteristics of the inputs and outputs on the user circuitry connector that are provided in "40-Pin User Circuitry Interface Connector Pinouts".

5.2 UART Timing

The UART interface supports:

- 8-bit data transfer
- 1 start bit
- Programmable stop bit(s): 1 or 2
- Parity: Even, odd, or none
- Baud rates:
  - Predefined rates: 9600, 14 400, 19 200, 28 800, 38 400, 57 600, 115 200, 230 400, 460 800, 921 600
  - Programmable
- Loop back mode from downstream to upstream



A number of preset baud rates can be used. If you require a baud rate that is not covered by the presets, you can specify your own baud rate. To specify your own baud rate:

1. In the **Device Control** dialog box, under **Port Communication**, choose **Programmable** in the **BulkBaudRate** list.
2. In the **BulkBaudRateFactor** field, enter a baud rate between 1 and 511.

The embedded video interface calculates the baud rate using the following equation: (66.66MHz * 1000000)/(BulkBaudRateFactor * 16)

Table 17: UART Baud Rates

Baud rate (BR) [bps]	Notes
9,600	Preset 0 (default)
14,400	Preset 1
19,200	Preset 2
28,800	Preset 3
38,400	Preset 4
57,600	Preset 5
115,200	Preset 6
230,400	Preset 7
460,800	Preset 8
921,600	Preset 9
Minimum: 4,166,667 Maximum: 8,154	Programmable baud rate

The following table lists the A.C. operating characteristics of the UART interface.

Table 18: A.C Operating Characteristics of the UART Interface

Parameter	Symbol	Minimum	Maximum	Units
Data period	$_{t}$UART	0.240	122.64	µs
Baud rate	BR	8,154	4,166,667	bps

5.3 USRT Timing

The USRT (Universal Synchronous Receiver/Transmitter) serial interface resembles the UART interface, but adds a clock signal to enable synchronous communication.

The following table lists the supported USRT clock frequencies and periods.

Table 19: Supported USRT Clock Frequencies and Periods

Bulk system clock divider	Clock period, tSCK (ns)	Clock frequency (MHz)*
By 2	60	16.667
By 4	120	8.333
By 8	240	4.167
By 16	480	2.083
By 32	960	1.042
By 64	1920	0.521
By 128	3840	0.260
By 256	7680	0.130

* To obtain the exact frequency, divide the 33.333 MHz clock speed by one of: 2, 4, 8, 16, 32, 64, 128, or 256.

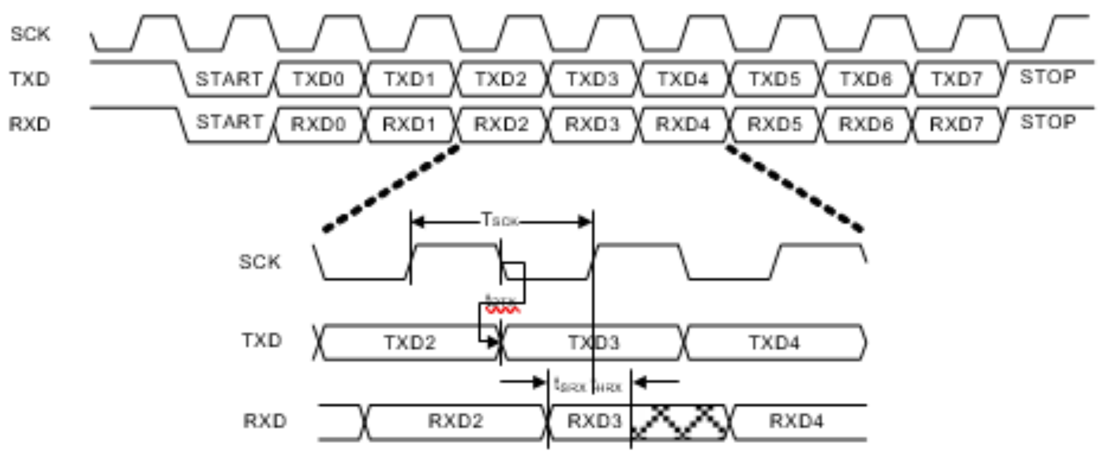


Table 20: USRT Delays

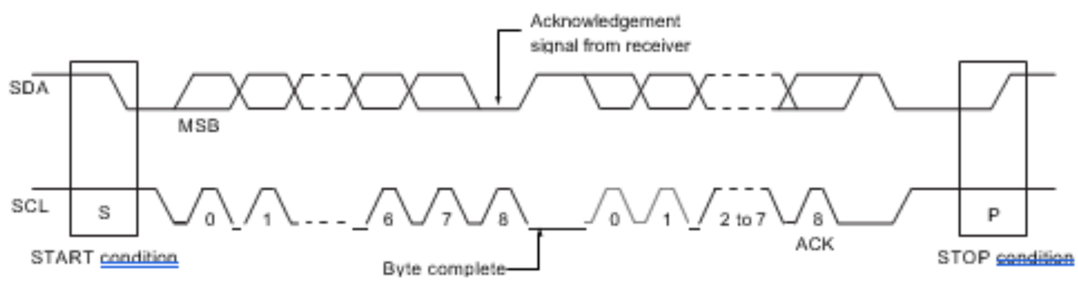
Delay	Minimum	Maximum
SCK to TXD delay tDTx	-12 ns	12 ns
RXD setup time tSRx	22 ns	N/A
RXD hold time tHRx	0 ns	N/A

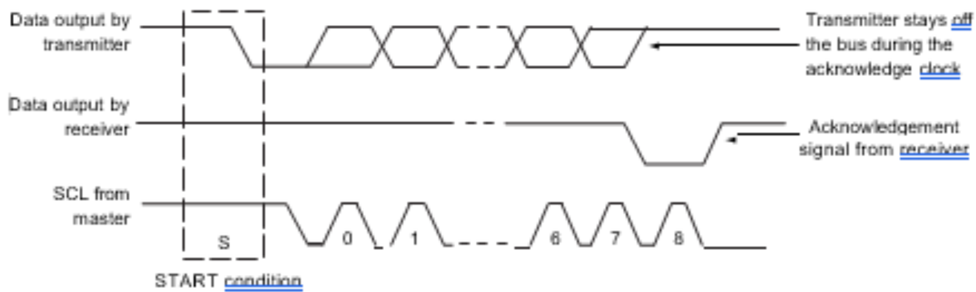
5.4 I2C Transmission Speeds

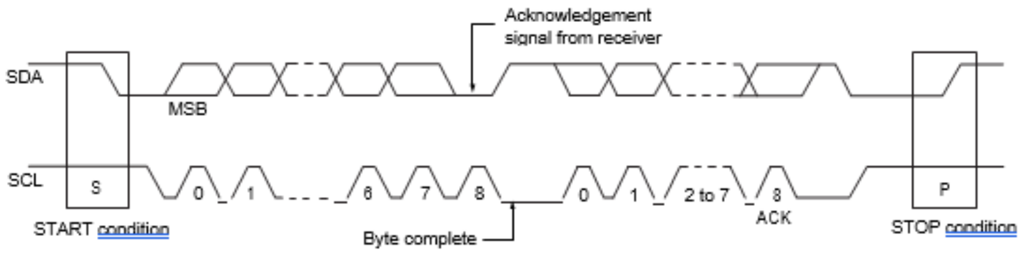
An I2C master mode is available that can be used to communicate with I2C slave devices. The I2C interface is a two-wire, bi-directional serial bus with a serial clock line (SCL) and a serial data line (SDA). Note that all devices connected to these signals must have open drain or open collector outputs. Both lines must be pulled up to 2.5V and chosen to satisfy the rise time of the I2C specification.

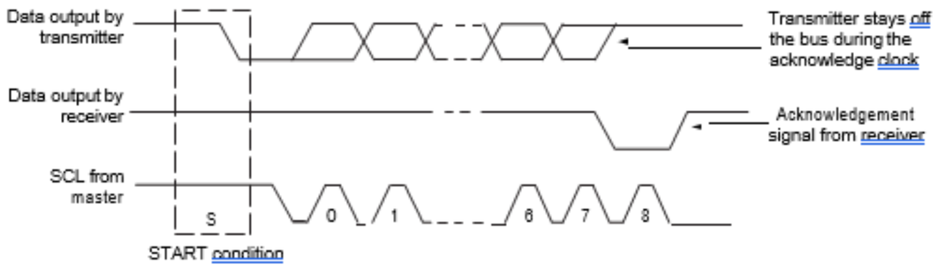
The embedded video interface is compatible with the Philips I2C standard and supports the following transmission speeds: Normal (100 kbit/s) and Fast (400 kbit/s).

Data is transferred synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is an SCL clock pulse for each data bit with the most significant bit (MSB) being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL.









5.5 SPI Signals

The NTx-Deca has an SPI master mode that is used to provide full duplex, synchronous serial communication using four wires. The master initiates the transaction by asserting slave select (SS). The master also drives a serial clock (SCLK) that provides a synchronous clock source to a slave device. The master transmits data on the Master Out Slave In (MOSI) line and receives data on the Master In Slave Out (MISO) line.

The SPI interface has the following characteristics:

- Master mode supports Motorola SPI protocol
- Programmable transfer rate using the **BulkSystemClockDivider** For more information, see "GenICam Interface for Serial Communication Configuration" .
    - Maximum value: 33.33 Mbps
    - Minimum value: 0.260 Mbps
- Serial clock with programmable phase and polarity
- SPI word length: 8, 10, 12, 14, and 16 bits
- Bit transmission: Most significant bit (msb) first

The following operating modes are supported:

Table 21: Supported SPI Operating Modes

SPI mode	Clock polarity (CPOL/CKP)	Clock phase (CPHA)
0	0	0

1	0	1
2	1	0
3	1	1

5.6 SPI Timing

The following table lists the supported SPI clock frequencies and periods.

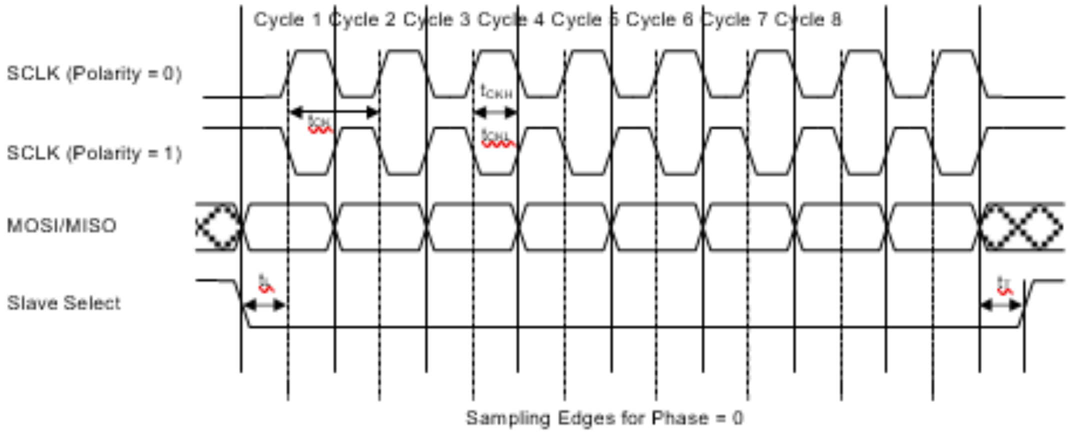
Table 22: Supported SPI Clock Frequencies and Periods

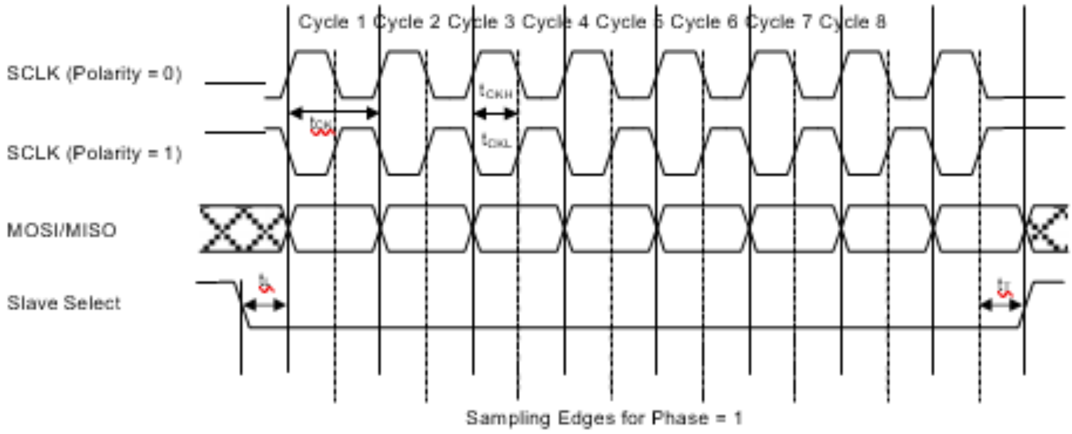
Bulk system clock divider	Clock period, tSCK (ns)	Clock frequency (MHz)*
By 2	30	33.333
By 4	60	16.667
By 8	120	8.333
By 16	240	4.167
By 32	480	2.083
By 64	960	1.042
By 128	1920	0.521
By 256	3840	0.260

*To obtain the exact frequency, divide the 66.66 MHz clock speed by one of: 2, 4, 8, 16, 32, 64, 128, or 256.

The SPI interface has four modes of operation based on two parameters: clock polarity and clock phase. The master and slave must use the same mode to communicate properly.

BulkSPIClockPolarity controls an active high or low clock. **BulkSPIClockPhase** controls how data should be launched or captured.





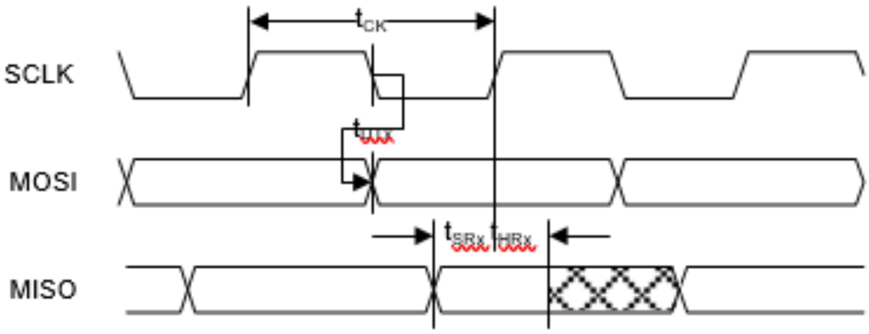


Table 23: SPI Delays

Delay	Minimum	Maximum
SPI transmit clock period ^{t}CK	30 ns	3840 ns

SPI transmit clock high pulse ^{t}CKH	15 ns	1920 ns
SPI transmit clock low pulse ^{t}CKL	15 ns	1920 ns
Leading time from slave select assertion to first clock edge ^{t}L	1/2 ^{t}CK	1/2 ^{t}CK
Trailing time from last clock edge to slave select deassertion ^{t}T	1/2 ^{t}CK	1/2 ^{t}CK
SCLK toMOSI delay ^{t}DTx	-12 ns	12 ns
MISO setup time ^{t}SRx	22ns	N/A
MISO hold time ^{t}HRx	0 ns	N/A

5.7 High Speed Download Signals

The NTx-Deca has a High Speed Download (HSD) mode that is used to provide high-speed output-only synchronous serial communication using four (DualHSD) or six (QuadHSD) wires. The master initiates the transaction by asserting slave select (SS). The master also drives a serial clock (SCLK) that provides a synchronous clock source to a slave device. The master transmits data on the SOUT lines.

The HSD interface has the following characteristics:

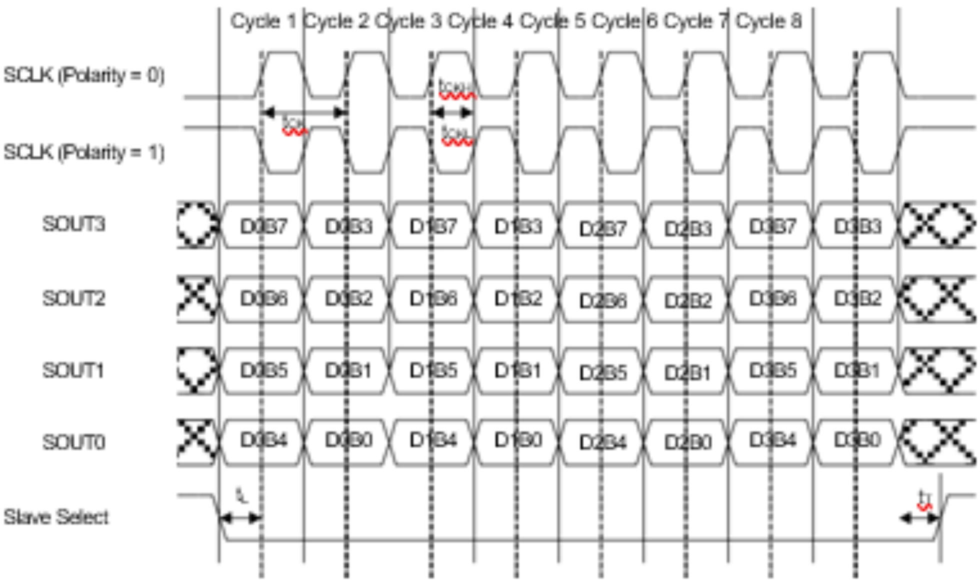
- Data transfer based on DualSPI and QuadSPI protocols, output-only
- Programmable transfer rate using the **BulkSystemClockDivider** For more information, see “GenICam Interface for Serial Communication Configuration”.
- Maximum value: 66 Mbps (DualHSD), 133.32 Mbps (QuadHSD)*
- Minimum value: 520 Mbps (DualHSD), 1.04 Mbps (QuadHSD)
- Serial clock with programmable phase and polarity
- HSD word length: 8 bits
- Bit transmission: Most significant bit (msb) first

5.8 High Speed Download Timing

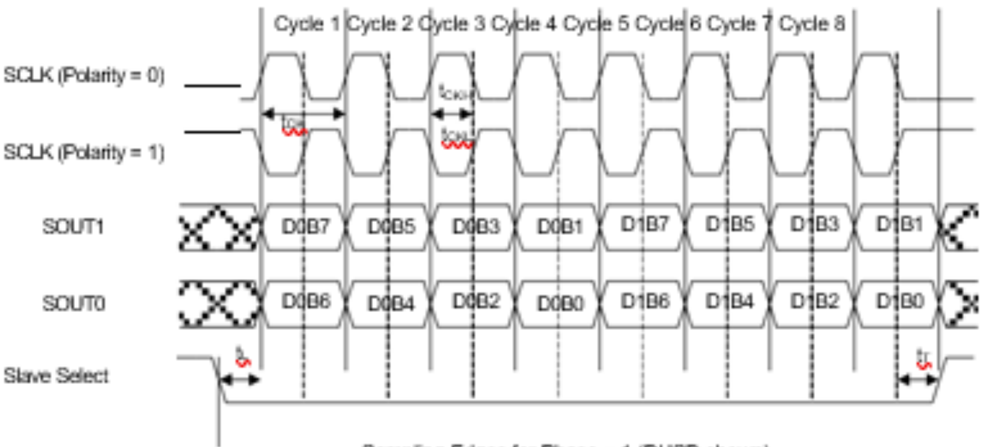
The clock frequencies and periods for the HSD clock are the same as the SPI clock frequencies. See Table 22: "Supported SPI Clock Frequencies and Periods".

The DualHSD (DHSD) bit rate is equal to two times the selected clock frequency, and the QuadHSD (QHSD) bit rate is equal to four times the selected clock frequency.

The HSD interface has four modes of operation based on two parameters: clock polarity and clock phase. The master and slave must use the same mode to communicate properly.



Sampling Edges for Phase = 0 (QHSD shown)



Sampling Edges for Phase = 1 (DHSD shown)

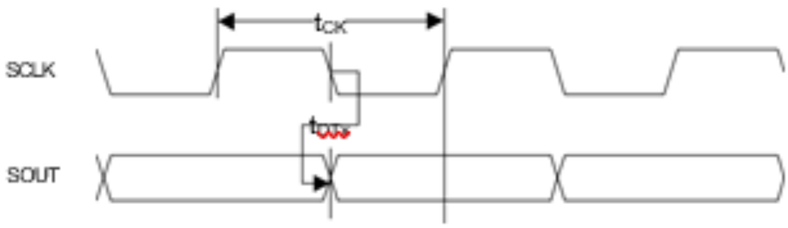


Table 24: HSD Delays

Delay	Minimum	Maximum
HSD transmit clock period ^{t}CK	30 ns	3840 ns

HSD transmit clock high pulse ^{t}CKH	15 ns	1920 ns
HSDtransmitclocklowpulsetCKL	15 ns	1920 ns
Leading time from slave select assertion to first clock edge ^{t}L	1/2 ^{t}CK	1/2 ^{t}CK
Trailing time from last clock edge to slave select deassertion ^{t}T	1/2 ^{t}CK	1/2 ^{t}CK
SCLK to SOUTn delay ^{t}DTx	-12 ns	12 ns

5.9 GenICam Interface for Serial Communication Configuration

The following GenICam features are available for serial communication configuration.

Table 25: GenICam Features Available for Serial Communication

Feature	Description
BulkSelector	Selects Bulk0 or Bulk1 for configuration.
BulkMode	UART/USRT/I2C/SPI/HSD protocol. Please note the following: • UART is available on all bulks • USRT is available on all bulks • I2C is available on all bulks • SPI is available on all bulks • DHSD is available when BulkSelector = Bulk0 • QHSD is available when BulkSelector = Bulk0
BulkSystemClockDivider	Defines the frequency of the USRT, SPI, DHSD, or QHSD output clock. The actual frequency produced is equal to the system clock frequency divided by the factor set by this feature. Available dividers are 2, 4, 8, 16, 32, 64, 128, and 256.

BulkOutputClockFrequency	Represents the frequency of the USRT, SPI, DHSD, or QHSD* output clock controlled by the BulkSystemClockDivider. The frequency is calculated using the following equation: • USRT: 33.33 MHz BulkSystemClockDivider • SPI, DHSD, and QHSD: 66.66 MHz BulkSystemClockDivider
BulkBaudRate	Selects a predefined baud rate or programmable option for the selected UART.
BulkBaudRateFactor	Programs a user defined baud rate for the selected UART.
BulkBaudRateValue	Displays the programmed baud rate for the selected UART.
BulkLoopback	Receives serial data sent from a host PC application to the video interface and loops it back to the host PC application. Available for UART or USRT only.
BulkNumOfStopBits	Selects a stop bit option (either 1 or 2). Available for UART or USRT only.
BulkParity	Selects a parity option (None, Even, or Odd). Available for UART or USRT only.
BulkUpstreamFifoWatermark	Sets the level of upstream FIFO at which a GigE Vision event is generated. This feature controls the number of bytes that can be accumulated in the bulk interface upstream FIFO before the embedded video interface delivers them to the host using an event type packet.
BulkSoftReset	Resets the bulk SPI, DHSD, and QHSD interface to the default settings.
BulkSPIClockPolarity	Selects the polarity of the SPI, DHSD, and QHSD clock.
BulkSPIClockPhase	Selects the phase of the SPI, DHSD, and QHSD clock.
BulkSPIWordSize	Controls the word size for a SPI transfer.

6 Sensor Interface

The NTx-Deca receives serialized pixel data and control signals from the sensor over the Low Voltage Differential Signaling (LVDS) interface, which it then deserializes.

This chapter describes the LVDS interface, including the expected pixel ordering in the sensor and LVDS timing requirements. It also describes how the deserializer is implemented in the embedded video interface.

At the end of this chapter you will find information about the pixel bus signals and timing values.

6.1 Low Voltage Differential Signaling (LVDS) Signals

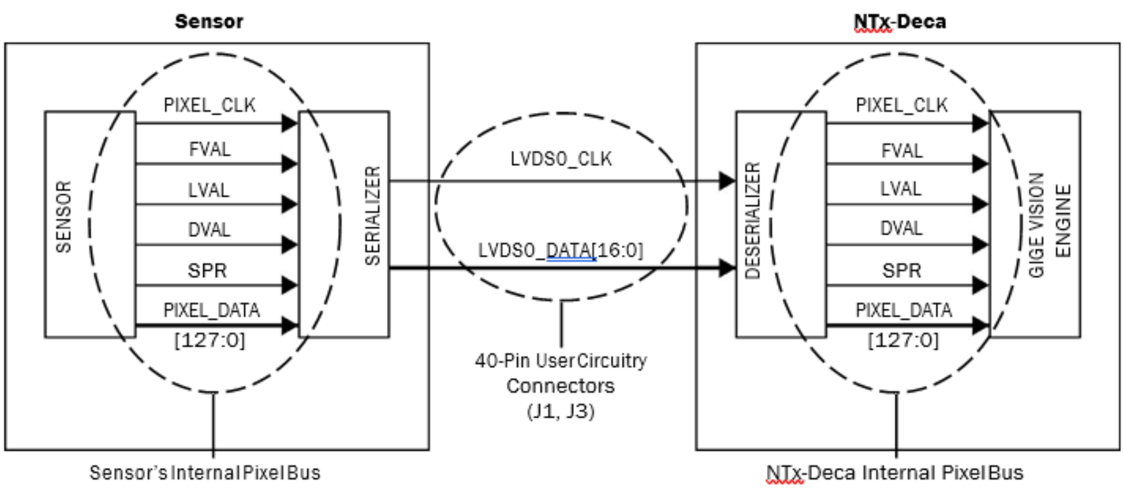
The NTx-Deca pixel bus has an 18-lane LVDS source synchronous interface. This interface includes:

- 17 LVDS pairs that are used for pixel data and control signals
- 1 LVDS pair that is used for clocking

The LVDS pairs are serialized and deserialized using an 8:1 ratio. The internal pixel bus before serialization (and after deserialization) is 136 bits wide. It includes:

- 128 bits for pixel data
- 4 bits for control data (frame (camera/sensor) synchronization)
- 4 unused bits (reserved for future use, not shown)

Figure 8: Serialization and Deserialization of Sensor Data



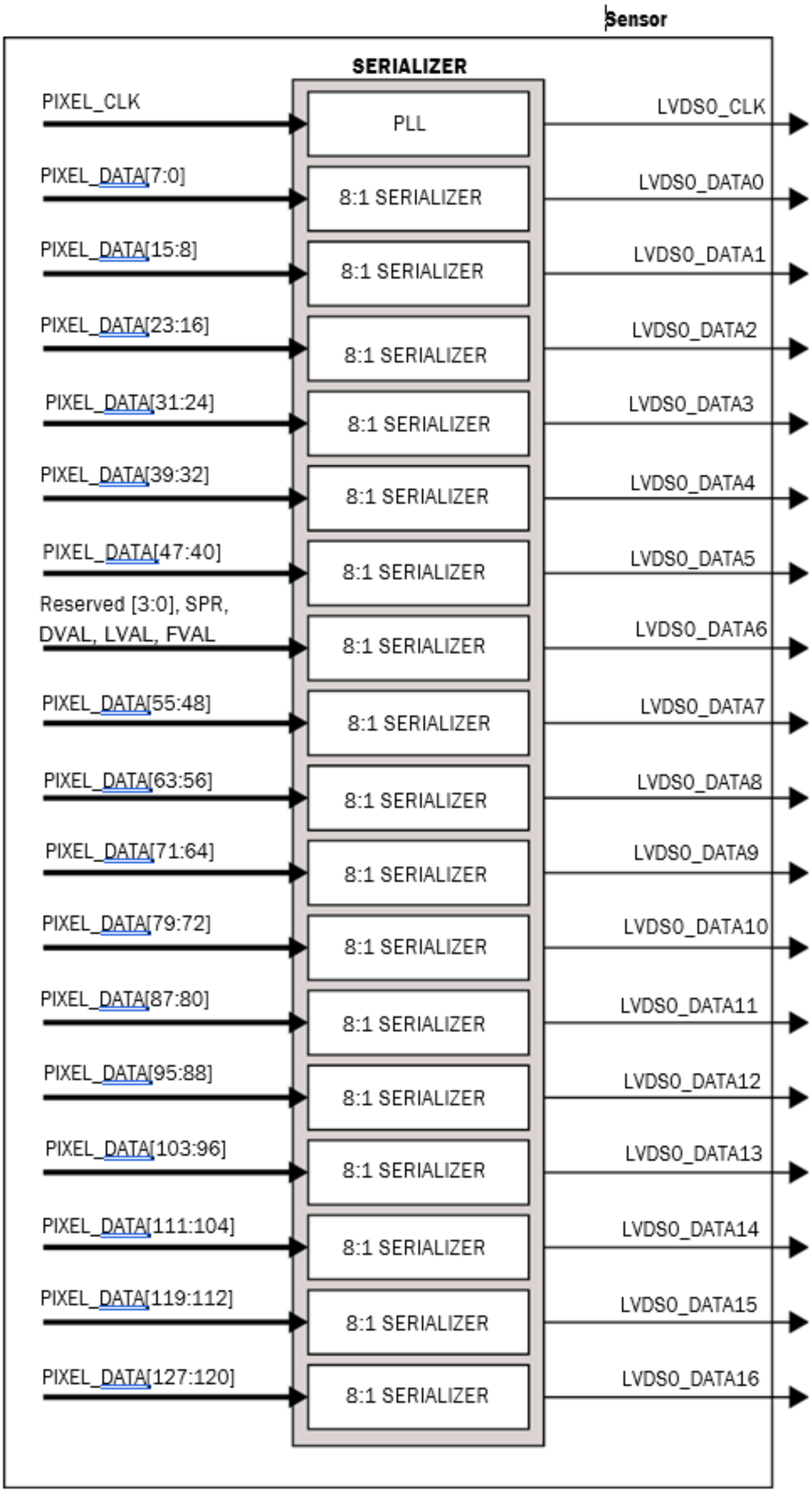
Note that the maximum parallel **PIXEL_CLK** frequency is 150 MHz, resulting in 1.2 Gbps LVDS data and a 150 MHz LVDS clock. As a result, the potential maximum pixel data throughput is 19.2 Gbps (128 bits x 150 MHz) which exceeds the maximum throughput of the 10G Ethernet interface.

The pinouts for the two user circuitry interfaces are provided in "40-Pin User Circuitry Interface Connector Pinouts".

6.1.1 LVDS Pixel Data Ordering

Figure 8 shows the parallel pixel bus coming from the sensor interface to the serializer to transmit pixel data across the LVDS interface. It is important that the sensor's serializer insert the pixel bits and control signals in the order shown below to ensure that they are reconstructed correctly in the NTx-Deca.

Figure 9: Pixel Ordering in the Sensor


Sensor
SERIALIZER
PIXEL_CLK
PLL
LVDS0_CLK
PIXEL_DATA[7:0]
8:1 SERIALIZER
LVDS0_DATA0
PIXEL_DATA[15:8]
8:1 SERIALIZER
LVDS0_DATA1
PIXEL_DATA[23:16]
8:1 SERIALIZER
LVDS0_DATA2
PIXEL_DATA[31:24]
8:1 SERIALIZER
LVDS0_DATA3
PIXEL_DATA[39:32]
8:1 SERIALIZER
LVDS0_DATA4
PIXEL_DATA[47:40]
8:1 SERIALIZER
LVDS0_DATA5
Reserved [3:0], SPR, DVAL, LVAL, FVAL
8:1 SERIALIZER
LVDS0_DATA6
PIXEL_DATA[55:48]
8:1 SERIALIZER
LVDS0_DATA7
PIXEL_DATA[63:56]
8:1 SERIALIZER
LVDS0_DATA8
PIXEL_DATA[71:64]
8:1 SERIALIZER
LVDS0_DATA9
PIXEL_DATA[79:72]
8:1 SERIALIZER
LVDS0_DATA10
PIXEL_DATA[87:80]
8:1 SERIALIZER
LVDS0_DATA11
PIXEL_DATA[95:88]
8:1 SERIALIZER
LVDS0_DATA12
PIXEL_DATA[103:96]
8:1 SERIALIZER
LVDS0_DATA13
PIXEL_DATA[111:104]
8:1 SERIALIZER
LVDS0_DATA14
PIXEL_DATA[119:112]
8:1 SERIALIZER
LVDS0_DATA15
PIXEL_DATA[127:120]
8:1 SERIALIZER
LVDS0_DATA16

The following timing diagram shows the bit mapping for the serialized data on the LVDS differential signals. The **LVDS0_DATA0** to **LVDS0_DATA5** pairs and **LVDS0_DATA7** to **LVDS0__DATA16** are used to transport pixel data, while the **LVDS0 DATA6** pair is used for frame (camera/sensor) synchronization.

Figure 10: LVDS Timing

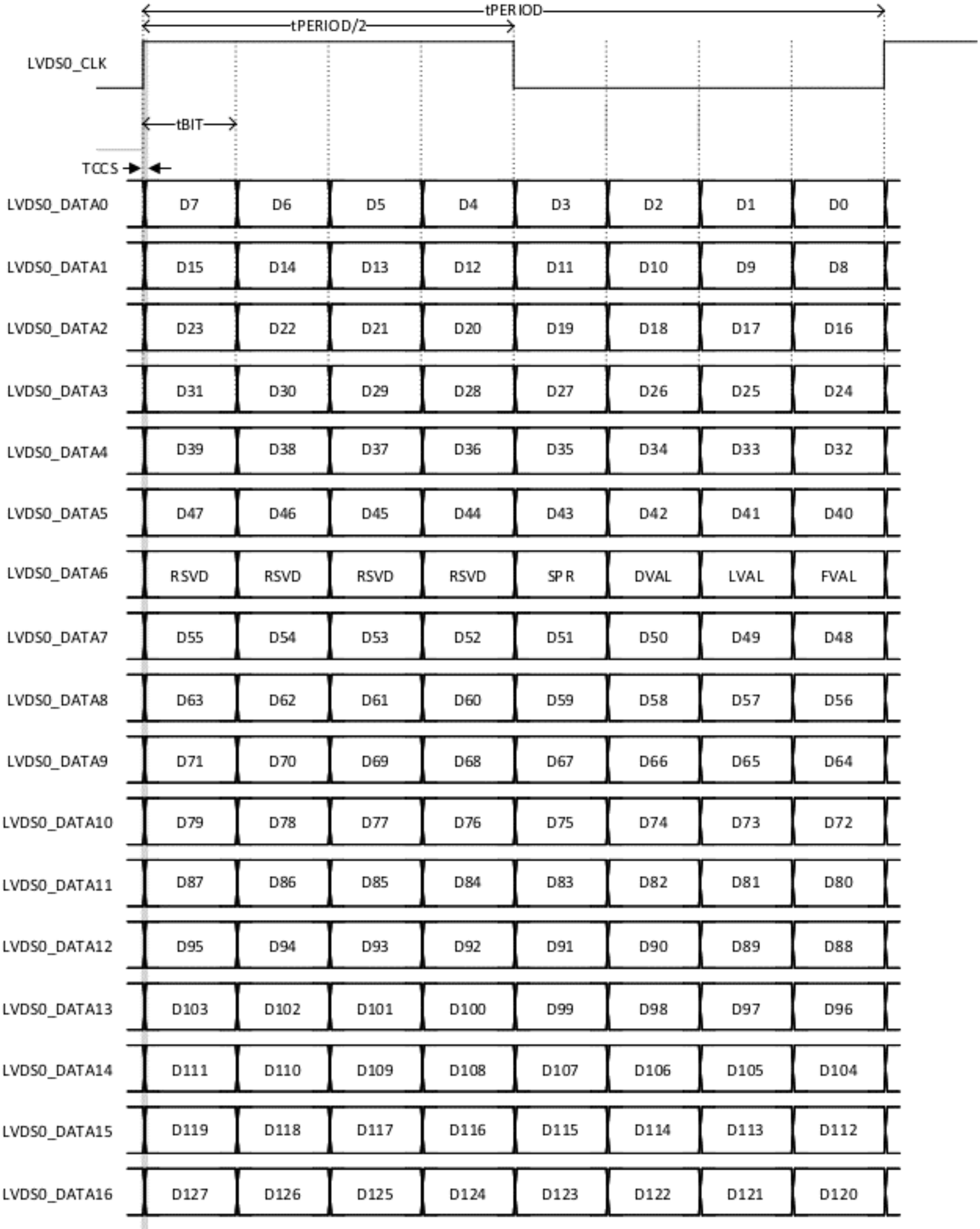


Table 26: LVDS Timing Information

Parameter	Minimum	Maximum
LVDS0_CLK frequency	37.5 MHz	150 MHz
LVDS0_CLK duty cycle	50%	
tPERIOD	26.7 ns	6.67 ns
tBIT	3.33 ns	834 ps
Transmitter Channel-to-Channel Skew (TCCS)	—	350 ps*

* This value represents the maximum allowed skew before user connectors (such as boards, cables, and the LVDS transmitter itself).

6.1.2 LVDS Input Standard Specifications

The NTx-Deca implements an LVDS deserializer inside the Xilinx Artix UltraScale+ FPGA. The LVDS signals that are received from the sensor must respect the Xilinx Artix UltraScale+ differential I/O must respect the Xilinx Artix UltraScale+ differential I/O standard as per reference document: DS931 - Artix UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics. This datasheet can be found on the AMD/Xilinx website: https://www.xilinx.com/products/silicon-devices/fpga.html.

Please refer to Table: LVDS DC Specifications.

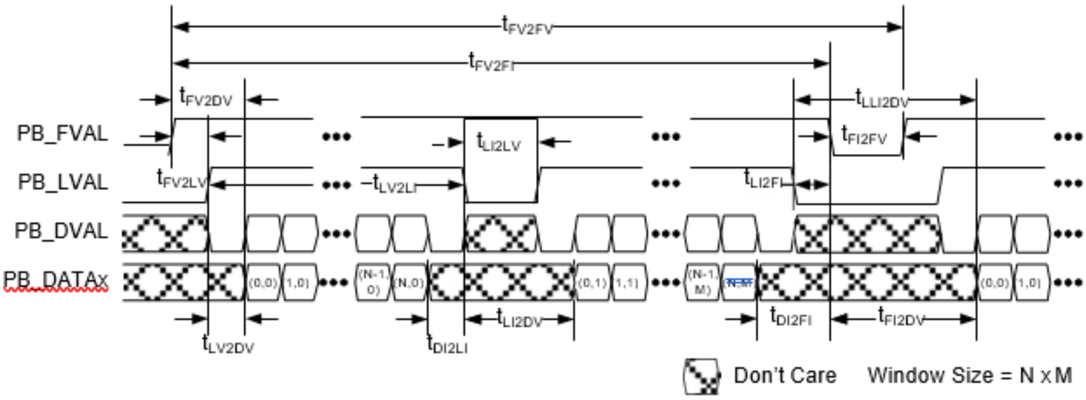
6.1.3 Limitations of the LVDS Clock

The LVDS clock (frequency) from the sensor should not be changed dynamically while the system is in operation. This could result in a reconfiguration of the internal deserializer and the loss of image data.

6.2 NTx-Deca Pixel Bus Timing

The output of the camera must match the format of the NTx-Deca. You should select a case for your application and then refer to "Timing Values for All Cases".

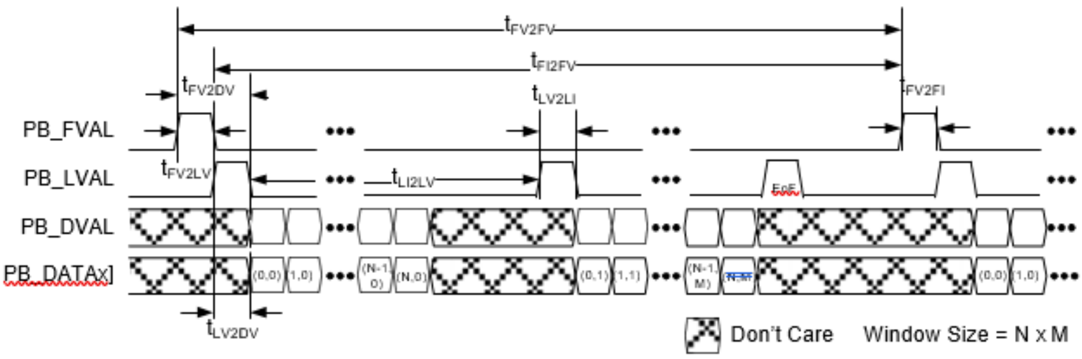
6.2.1 Case 1: FVAL and LVAL are Level-Sensitive



6.2.2 Case 2: FVAL and LVAL are Edge-Sensitive

In this case, FVAL and LVAL are edge-sensitive.

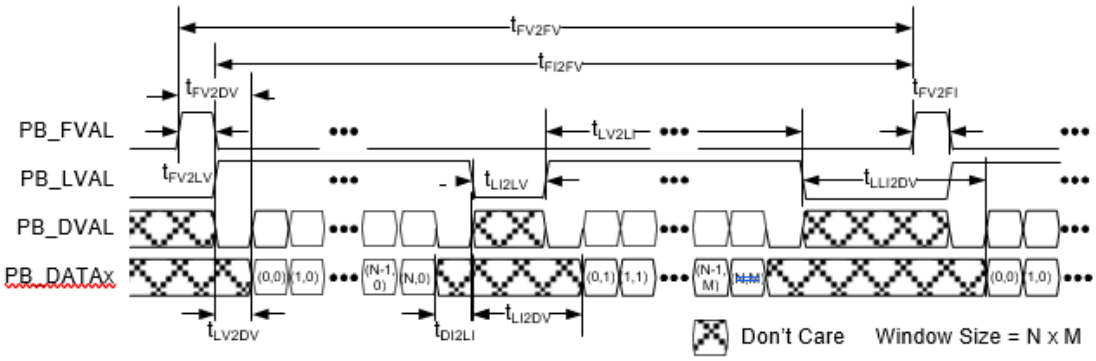
- **Start of frame/line is signaled by:** A rising (or falling) edge on FVAL, which signals the start of a *frame*. A rising (or falling) edge on LVAL, which signals the start of a *line*.
- End of frame is signaled by:
  - The next FVAL valid edge (rising edge when rising-edge sensitive or falling edge when falling-edge sensitive)
  - Or, when all of the pixels have been acquired (as set in the image height and width settings) **AND** an end-of-frame (EOF) occurs.
    Note: EOF occurs at LVAL rising edge (when rising-edge sensitive) or LVAL falling edge (when falling-edge sensitive). This is an additional LVAL edge, in addition to the configured/expected number of lines. See the EOF indicator in the illustration below.
- **Line Missing status and Partial Line Missing errors:** Partial Line Missing indicates lines are ending early (the next LVAL valid edge occurs before all of the pixels have been acquired). Full Line Missing indicates that the frame is ending early (the next FVAL edge occurs before all of the lines have been acquired).



6.2.3 Case 3: FVAL is Edge-Sensitive and LVAL is Level-Sensitive

In this case, FVAL is edge-sensitive and LVAL is level-sensitive.

- **Start of frame/line is signaled by:** A rising (or falling) edge on FVAL, which signals start of *frame*. The line is valid when LVAL is active (high or low depending on settings).
- End of frame is signaled by:
  - The next FVAL valid edge (rising edge when rising-edge sensitive or falling edge when falling-edge sensitive)
  - Or when all of the lines have been acquired (as set in the image height settings) **AND** the last LVAL with valid data is de-asserted (low when high level sensitive or high when low level sensitive).
- Line Missing status or a Partial Line Missing error generated:
  - Full Line Missing indicates that the frame is ending early (the next FVAL edge occurs before all of the lines have been acquired). Partial Line Missing indicates that lines are ending early (in this case, LVAL is de-asserted before all pixels in a line are captured).



6.2.4 Timing Values for All Cases

The TCP (PB_CLK period) timing values listed in the following table are minimum values only.

Table 27: TCP Timing Values for All Cases

From	To	Symbol	Case 1 (level) (tcp)	Case 2 (edge) (tcp)	Case 3 (both) (tcp)
FVAL valid	LVAL valid [a]	tFV2LV	0 [b]	0	1
FVAL valid	Data valid [a,c,d]	tFV2DV	0 [b]	16 [f]	1

LVAL valid	Data valid [a,c,d]	tLV2DV	0	1	0
LVAL valid	LVAL invalid [a]	tLV2LI	1	1	1
LVAL invalid	LVAL valid [a]	tLI2LV	1	1	1
LVAL invalid (Automatic Internal Retrigger disabled)	Data valid [a,c,d]	tLI2DV	1	N/A	1
LVAL invalid (Automatic Internal Retrigger enabled)	Data valid	tLI2DV	16[g]	N/A	16[g]
Data invalid	LVAL invalid [a,c,d]	tDI2LI	0	N/A	0
LVAL invalid	FVAL invalid [a]	tLI2FI	0[e]	N/A	N/A
Data invalid	FVAL invalid [a,c,d]	tDI2FI	0[e]	N/A	N/A
FVAL invalid	FVAL valid [a]	tFI2FV	1	1	1
FVAL invalid	Data valid [a,c,d]	tFI2DV	1	N/A	N/A
Last LVAL invalid	Data valid	tLLI2DV	16 [f]	N/A	16 [f]
FVAL valid	FVAL invalid	tFV2FI	16 [f]	1	1
FVAL valid	FVAL valid	t2FV2FV	17 [f]	17 [f]	17 [f]

a. The valid state of FVAL and LVAL is high when they are set as level-high sensitive or rising-edge sensitive. Their valid state is low when they are set as level-low sensitive or falling-edge sensitive.

b. If LVAL is valid before FVAL becomes valid, the grabber drops the full line.

c. Data valid is defined by FVAL valid (note a), LVAL valid (note a), and DVAL valid (note d).

d. The valid state of DVAL is high when it is set as level-high sensitive, and low when set as level-low sensitive. DVAL is always valid in the grabber when the **PixelBusDataValidEnabled** feature is off.

e. If FVAL becomes invalid and LVAL is still valid, the line is truncated.

f. This is a worst-case Subtract 3 cycles if the pixel type is 8-bit, 1-tap. Subtract 1 cycle for all other pixel types except 10/12- bit, 2-tap, unpacked, and RGB unpacked. Subtract up to 7 cycles if the image size is a multiple of 32 bytes.

6.3 Pixel Bus Bit Map

The following tables show how the pixel bus signals are ordered, based on the available pixel formats.

6.3.1 Color Filters

Table 28: Mono/Bayer/SCF/RGB8 Color Filters

	Mono8/ Bayer8/ SCF1_8 *		Mono10/ Bayer10/ SCF1_10 *		Mono12/ Bayer12/ SCF1_12 *		Mono14		Mono16/ Bayer16		Mono16/ Bayer16		RGB8		
	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Comp	Bit
PB0_DATA00	0	0	0	0	0	0	0	0	0	0	0	0	0	R	0
PB0_DATA01	0	1	0	1	0	1	0	1	0	1	0	1	0	R	1
PB0_DATA02	0	2	0	2	0	2	0	2	0	2	0	2	0	R	2
PB0_DATA03	0	3	0	3	0	3	0	3	0	3	0	3	0	R	3
PB0_DATA04	0	4	0	4	0	4	0	4	0	4	0	4	0	R	4
PB0_DATA05	0	5	0	5	0	5	0	5	0	5	0	5	0	R	5
PB0_DATA06	0	6	0	6	0	6	0	6	0	6	0	6	0	R	6

PB0_DATA07	0	7	0	7	0	7	0	7	0	7	0	7	0	R	7
PB0_DATA08	1	0	0	8	0	8	0	8	0	8	0	8	0	G	0
PB0_DATA09	1	1	0	9	0	9	0	9	0	9	0	9	0	G	1
PB0_DATA10	1	2	nc	nc	0	10	0	10	0	10	0	10	0	G	2
PB0_DATA11	1	3	nc	nc	0	11	0	11	0	11	0	11	0	G	3
PB0_DATA12	1	4	1	8	1	8	0	12	0	12	0	12	0	G	4
PB0_DATA13	1	5	1	9	1	9	0	13	0	13	0	13	0	G	5
PB0_DATA14	1	6	nc	nc	1	10	nc	nc	0	14	0	14	0	G	6
PB0_DATA15	1	7	nc	nc	1	11	nc	nc	0	15	0	15	0	G	7
PB0_DATA16	2	0	1	0	1	0	1	0	1	0	0	16	0	B	0
PB0_DATA17	2	1	1	1	1	1	1	1	1	1	0	17	0	B	1
PB0_DATA18	2	2	1	2	1	2	1	2	1	2	0	18	0	B	2
PB0_DATA19	2	3	1	3	1	3	1	3	1	3	0	19	0	B	3
PB0_DATA20	2	4	1	4	1	4	1	4	1	4	0	20	0	B	4

Table 28: Mono/Bayer/SCF/RGB8 Color Filters (Continued)

	Mono8/ Bayer8/ SCF1_8 *		Mono10/ Bayer10/ SCF1_10 *		Mono12/ Bayer12/ SCF1_12 *		Mono14		Mono16/ Bayer16		Mono16/ Bayer16		RGB8		
	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Comp	Bit
PB0_DATA21	2	5	1	5	1	5	1	5	1	5	0	21	0	B	5
PB0_DATA22	2	6	1	6	1	6	1	6	1	6	0	22	0	B	6
PB0_DATA23	2	7	1	7	1	7	1	7	1	7	0	23	0	B	7
PB0_DATA24	3	0	3	0	3	0	1	8	1	8	0	24	1	R	0
PB0_DATA25	3	1	3	1	3	1	1	9	1	9	0	25	1	R	1
PB0_DATA26	3	2	3	2	3	2	1	10	1	10	0	26	1	R	2
PB0_DATA27	3	3	3	3	3	3	1	11	1	11	0	27	1	R	3
PB0_DATA28	3	4	3	4	3	4	1	12	1	12	0	28	1	R	4
PB0_DATA29	3	5	3	5	3	5	1	13	1	13	0	29	1	R	5
PB0_DATA30	3	6	3	6	3	6	nc	nc	1	14	0	30	1	R	6
PB0_DATA31	3	7	3	7	3	7	nc	nc	1	15	0	31	1	R	7
PB0_DATA32	4	0	2	0	2	0	2	0	2	0	1	0	1	G	0

PB0_DATA33	4	1	2	1	2	1	2	1	2	1	1	1	1	G	1
PB0_DATA34	4	2	2	2	2	2	2	2	2	2	1	2	1	G	2
PB0_DATA35	4	3	2	3	2	3	2	3	2	3	1	3	1	G	3
PB0_DATA36	4	4	2	4	2	4	2	4	2	4	1	4	1	G	4
PB0_DATA37	4	5	2	5	2	5	2	5	2	5	1	5	1	G	5
PB0_DATA38	4	6	2	6	2	6	2	6	2	6	1	6	1	G	6
PB0_DATA39	4	7	2	7	2	7	2	7	2	7	1	7	1	G	7
PB0_DATA40	5	0	2	8	2	8	2	8	2	8	1	8	1	B	0

Table 28: Mono/Bayer/SCF/RGB8 Color Filters (Continued)

	Mono8/ Bayer8/ SCF1_8 *		Mono10/ Bayer10/ SCF1_10 *		Mono12/ Bayer12/ SCF1_12 *		Mono14		Mono16/ Bayer16		Mono32		RGB8		
	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Comp	Bit
PB0_DATA41	5	1	2	9	2	9	2	9	2	9	1	9	1	B	1
PB0_DATA42	5	2	nc	nc	2	10	2	10	2	10	1	10	1	B	2

PB0_DATA43	5	3	nc	nc	2	11	2	11	2	11	1	11	1	B	3
PB0_DATA44	5	4	3	8	3	8	2	12	2	12	1	12	1	B	4
PB0_DATA45	5	5	3	9	3	9	2	13	2	13	1	13	1	B	5
PB0_DATA46	5	6	nc	nc	3	10	nc	nc	2	14	1	14	1	B	6
PB0_DATA47	5	7	nc	nc	3	11	nc	nc	2	15	1	15	1	B	7
PB0_DATA48	6	0	4	0	4	0	3	0	3	0	1	16	nc	nc	nc
PB0_DATA49	6	1	4	1	4	1	3	1	3	1	1	17	nc	nc	nc
PB0_DATA50	6	2	4	2	4	2	3	2	3	2	1	18	nc	nc	nc
PB0_DATA51	6	3	4	3	4	3	3	3	3	3	1	19	nc	nc	nc
PB0_DATA52	6	4	4	4	4	4	3	4	3	4	1	20	nc	nc	nc
PB0_DATA53	6	5	4	5	4	5	3	5	3	5	1	21	nc	nc	nc

PB0_DATA54	6	6	4	6	4	6	3	6	3	6	1	22	nc	nc	nc
PB0_DATA55	6	7	4	7	4	7	3	7	3	7	1	23	nc	nc	nc
PB0_DATA56	7	0	4	8	4	8	3	8	3	8	1	24	nc	nc	nc
PB0_DATA57	7	1	4	9	4	9	3	9	3	9	1	25	nc	nc	nc
PB0_DATA58	7	2	nc	nc	4	10	3	10	3	10	1	26	nc	nc	nc
PB0_DATA59	7	3	nc	nc	4	11	3	11	3	11	1	27	nc	nc	nc
PB0_DATA60	7	4	5	8	5	8	3	12	3	12	1	28	nc	nc	nc

Table 28: Mono/Bayer/SCF/RGB8 Color Filters (Continued)

	Mono8/ Bayer8/ SCF1_8 *		Mono10/ Bayer10/ SCF1_10 *		Mono12/ Bayer12/ SCF1_12 *		Mono14		Mono16/ Bayer16		Mono32		RGB8		
	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Comp	Bit
PB0_DATA61	7	5	5	9	5	9	3	13	3	13	1	29	nc	nc	nc

PB0_DATA62	7	6	nc	nc	5	10	nc	nc	3	14	1	30	nc	nc	nc
PB0_DATA63	7	7	nc	nc	5	11	nc	nc	3	15	1	31	nc	nc	nc
PB0_DATA64	8	0	5	0	5	0	4	0	4	0	2	0	nc	nc	nc
PB0_DATA65	8	1	5	1	5	1	4	1	4	1	2	1	nc	nc	nc
PB0_DATA66	8	2	5	2	5	2	4	2	4	2	2	2	nc	nc	nc
PB0_DATA67	8	3	5	3	5	3	4	3	4	3	2	3	nc	nc	nc
PB0_DATA68	8	4	5	4	5	4	4	4	4	4	2	4	nc	nc	nc
PB0_DATA69	8	5	5	5	5	5	4	5	4	5	2	5	nc	nc	nc
PB0_DATA70	8	6	5	6	5	6	4	6	4	6	2	6	nc	nc	nc
PB0_DATA71	8	7	5	7	5	7	4	7	4	7	2	7	nc	nc	nc
PB0_DATA72	9	0	7	0	7	8	4	8	4	8	2	8	nc	nc	nc

PB0_DATA73	9	1	7	1	7	9	4	9	4	9	2	9	nc	nc	nc
PB0_DATA74	9	2	7	2	7	10	4	10	4	10	2	10	nc	nc	nc
PB0_DATA75	9	3	7	3	7	11	4	11	4	11	2	11	nc	nc	nc
PB0_DATA76	9	4	7	4	7	12	4	12	4	12	2	12	nc	nc	nc
PB0_DATA77	9	5	7	5	7	13	4	13	4	13	2	13	nc	nc	nc
PB0_DATA78	9	6	7	6	7	14	nc	nc	4	14	2	14	nc	nc	nc
PB0_DATA79	9	7	7	7	7	15	nc	nc	4	15	2	15	nc	nc	nc
PB0_DATA80	nc	nc	6	0	6	0	5	0	5	0	2	16	nc	nc	nc

Table 28: Mono/Bayer/SCF/RGB8 Color Filters (Continued)

	Mono8/ Bayer8/ SCF1_8 *		Mono10/ Bayer10/ SCF1_10 *		Mono12/ Bayer12/ SCF1_12 *		Mono14		Mono16/ Bayer16		Mono32		RGB8		
	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Comp	Bit
PB0_DATA81	nc	nc	6	1	6	1	5	1	5	1	2	17	nc	nc	nc

PB0_DATA82	nc	nc	6	2	6	2	5	2	5	2	2	18	nc	nc	nc
PB0_DATA83	nc	nc	6	3	6	3	5	3	5	3	2	19	nc	nc	nc
PB0_DATA84	nc	nc	6	4	6	4	5	4	5	4	2	20	nc	nc	nc
PB0_DATA85	nc	nc	6	5	6	5	5	5	5	5	2	21	nc	nc	nc
PB0_DATA86	nc	nc	6	6	6	6	5	6	5	6	2	22	nc	nc	nc
PB0_DATA87	nc	nc	6	7	6	7	5	7	5	7	2	23	nc	nc	nc
PB0_DATA88	nc	nc	6	8	6	8	5	8	5	8	2	24	nc	nc	nc
PB0_DATA89	nc	nc	6	9	6	9	5	9	5	9	2	25	nc	nc	nc
PB0_DATA90	nc	nc	nc	nc	6	10	5	10	5	10	2	26	nc	nc	nc
PB0_DATA91	nc	nc	nc	nc	6	11	5	11	5	11	2	27	nc	nc	nc
PB0_DATA92	nc	nc	7	8	7	8	5	12	5	12	2	28	nc	nc	nc
PB0_DATA93	nc	nc	7	9	7	9	5	13	5	13	2	29	nc	nc	nc
PB0_DATA94	nc	nc	nc	nc	7	10	nc	nc	5	14	2	30	nc	nc	nc
PB0_DATA95	nc	nc	nc	nc	7	11	nc	nc	5	15	2	31	nc	nc	nc

PB0_DATA96	nc	nc	nc	nc	nc	nc	6	0	6	0	3	0	nc	nc	nc
PB0_DATA97	nc	nc	nc	nc	nc	nc	6	1	6	1	3	1	nc	nc	nc
PB0_DATA98	nc	nc	nc	nc	nc	nc	6	2	6	2	3	2	nc	nc	nc
PB0_DATA99	nc	nc	nc	nc	nc	nc	6	3	6	3	3	3	nc	nc	nc
PB0_DATA100	nc	nc	nc	nc	nc	nc	6	4	6	4	3	4	nc	nc	nc

Table 28: Mono/Bayer/SCF/RGB8 Color Filters (Continued)

	Mono8/ Bayer8/ SCF1_8 *		Mono10/ Bayer10/ SCF1_10 *		Mono12/ Bayer12/ SCF1_12 *		Mono14		Mono16/ Bayer16		Mono32		RGB8		
	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Comp	Bit
PB0_DATA101	nc	nc	nc	nc	nc	nc	6	5	6	5	3	5	nc	nc	nc
PB0_DATA102	nc	nc	nc	nc	nc	nc	6	6	6	6	3	6	nc	nc	nc
PB0_DATA103	nc	nc	nc	nc	nc	nc	6	7	6	7	3	7	nc	nc	nc
PB0_DATA104	nc	nc	nc	nc	nc	nc	6	8	6	8	3	8	nc	nc	nc

PB0_DATA105	nc	nc	nc	nc	nc	nc	6	9	6	9	3	9	nc	nc	nc
PB0_DATA106	nc	nc	nc	nc	nc	nc	6	10	6	10	3	10	nc	nc	nc
PB0_DATA107	nc	nc	nc	nc	nc	nc	6	11	6	11	3	11	nc	nc	nc
PB0_DATA108	nc	nc	nc	nc	nc	nc	6	12	6	12	3	12	nc	nc	nc
PB0_DATA109	nc	nc	nc	nc	nc	nc	6	13	6	13	3	13	nc	nc	nc
PB0_DATA110	nc	nc	nc	nc	nc	nc	nc	nc	6	14	3	14	nc	nc	nc
PB0_DATA111	nc	nc	nc	nc	nc	nc	nc	nc	6	15	3	15	nc	nc	nc
PB0_DATA112	nc	nc	nc	nc	nc	nc	7	0	7	0	3	16	nc	nc	nc
PB0_DATA113	nc	nc	nc	nc	nc	nc	7	1	7	1	3	17	nc	nc	nc
PB0_DATA114	nc	nc	nc	nc	nc	nc	7	2	7	2	3	18	nc	nc	nc
PB0_DATA115	nc	nc	nc	nc	nc	nc	7	3	7	3	3	19	nc	nc	nc

PB0_DATA116	nc	nc	nc	nc	nc	nc	7	4	7	4	3	20	nc	nc	nc
PB0_DATA117	nc	nc	nc	nc	nc	nc	7	5	7	5	3	21	nc	nc	nc
PB0_DATA118	nc	nc	nc	nc	nc	nc	7	6	7	6	3	22	nc	nc	nc
PB0_DATA119	nc	nc	nc	nc	nc	nc	7	7	7	7	3	23	nc	nc	nc
PB0_DATA120	nc	nc	nc	nc	nc	nc	7	8	7	8	3	24	nc	nc	nc

Table 28: Mono/Bayer/SCF/RGB8 Color Filters (Continued)

	Mono8/ Bayer8/ SCF1_8 *		Mono10/ Bayer10/ SCF1_10 *		Mono12/ Bayer12/ SCF1_12 *		Mono14		Mono16 / Bayer16		Mono32		RGB8		
	Tap	**Bit**	**Tap**	**Bit**	**Tap**	**Bit**	**Tap**	**Bit**	**Tap**	**Bit**	**Tap**	**Bit**	**Tap**	**Comp**	**Bit**
PB0_DATA121	nc	nc	nc	nc	nc	nc	7	9	7	9	3	25	nc	nc	nc
PB0_DATA122	nc	nc	nc	nc	nc	nc	7	10	7	10	3	26	nc	nc	nc
PB0_DATA123	nc	nc	nc	nc	nc	nc	7	11	7	11	3	27	nc	nc	nc
PB0_DATA124	nc	nc	nc	nc	nc	nc	7	12	7	12	3	28	nc	nc	nc
PB0_DATA125	nc	nc	nc	nc	nc	nc	7	13	7	13	3	29	nc	nc	nc

PB0_DATA126	nc	nc	nc	nc	nc	nc	nc	nc	7	14	3	30	nc	nc	nc
PB0_DATA127	nc	nc	nc	nc	nc	nc	nc	nc	7	15	3	31	nc	nc	nc

SCF1_8, SCF1_10 and SCF1_12 is for SCF1WGWR8, SCF1WGWR10 and SCF1WGWR12.

Table 29: BGR8/YUV8_UYV/RGBA8/BGRA8/RGB10 Color Filters

	BGR8			YUV8_UYV			RGBA8			BGRA8			RGB10		
	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA00	0	B	0	0	U	0	0	R	0	0	B	0	0	R	0
PB0_DATA01	0	B	1	0	U	1	0	R	1	0	B	1	0	R	1
PB0_DATA02	0	B	2	0	U	2	0	R	2	0	B	2	0	R	2
PB0_DATA03	0	B	3	0	U	3	0	R	3	0	B	3	0	R	3
PB0_DATA04	0	B	4	0	U	4	0	R	4	0	B	4	0	R	4
PB0_DATA05	0	B	5	0	U	5	0	R	5	0	B	5	0	R	5
PB0_DATA06	0	B	6	0	U	6	0	R	6	0	B	6	0	R	6
PB0_DATA07	0	B	7	0	U	7	0	R	7	0	B	7	0	R	7
PB0_DATA08	0	G	0	0	Y	0	0	G	0	0	G	0	0	R	8

PB0_DATA09	0	G	1	0	Y	1	0	G	1	0	G	1	0	R	9
PB0_DATA10	0	G	2	0	Y	2	0	G	2	0	G	2	nc	nc	nc
PB0_DATA11	0	G	3	0	Y	3	0	G	3	0	G	3	nc	nc	nc
PB0_DATA12	0	G	4	0	Y	4	0	G	4	0	G	4	0	B	8
PB0_DATA13	0	G	5	0	Y	5	0	G	5	0	G	5	0	B	9
PB0_DATA14	0	G	6	0	Y	6	0	G	6	0	G	6	nc	nc	nc
PB0_DATA15	0	G	7	0	Y	7	0	G	7	0	G	7	nc	nc	nc
PB0_DATA16	0	R	0	0	V	0	0	B	0	0	R	0	0	B	0
PB0_DATA17	0	R	1	0	V	1	0	B	1	0	R	1	0	B	1
PB0_DATA18	0	R	2	0	V	2	0	B	2	0	R	2	0	B	2
PB0_DATA19	0	R	3	0	V	3	0	B	3	0	R	3	0	B	3
PB0_DATA20	0	R	4	0	V	4	0	B	4	0	R	4	0	B	4

Table 29: BGR8/YUV8_UYV/RGBA8/BGRA8/RGB10 Color Filters (Continued)

	BGR8			YUV8_UYV			RGBA8			BGRA8			RGB10		
	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit

PB0_DATA21	0	R	5	0	V	5	0	B	5	0	R	5	0	B	5
PB0_DATA22	0	R	6	0	V	6	0	B	6	0	R	6	0	B	6
PB0_DATA23	0	R	7	0	V	7	0	B	7	0	R	7	0	B	7
PB0_DATA24	1	B	0	1	U	0	0	A	0	0	A	0	1	R	0
PB0_DATA25	1	B	1	1	U	1	0	A	1	0	A	1	1	R	1
PB0_DATA26	1	B	2	1	U	2	0	A	2	0	A	2	1	R	2
PB0_DATA27	1	B	3	1	U	3	0	A	3	0	A	3	1	R	3
PB0_DATA28	1	B	4	1	U	4	0	A	4	0	A	4	1	R	4
PB0_DATA29	1	B	5	1	U	5	0	A	5	0	A	5	1	R	5
PB0_DATA30	1	B	6	1	U	6	0	A	6	0	A	6	1	R	6
PB0_DATA31	1	B	7	1	U	7	0	A	7	0	A	7	1	R	7
PB0_DATA32	1	G	0	1	Y	0	1	R	0	1	B	0	0	G	0
PB0_DATA33	1	G	1	1	Y	1	1	R	1	1	B	1	0	G	1
PB0_DATA34	1	G	2	1	Y	2	1	R	2	1	B	2	0	G	2

PB0_DATA35	1	G	3	1	Y	3	1	R	3	1	B	3	0	G	3
PB0_DATA36	1	G	4	1	Y	4	1	R	4	1	B	4	0	G	4
PB0_DATA37	1	G	5	1	Y	5	1	R	5	1	B	5	0	G	5
PB0_DATA38	1	G	6	1	Y	6	1	R	6	1	B	6	0	G	6
PB0_DATA39	1	G	7	1	Y	7	1	R	7	1	B	7	0	G	7
PB0_DATA40	1	R	0	1	V	0	1	G	0	1	G	0	0	G	8

Table 29: BGR8/YUV8_UYV/RGBA8/BGRA8/RGB10 Color Filters (Continued)

	BGR8			YUV8_UYV			RGBA8			BGRA8			RGB10		
	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA41	1	R	1	1	V	1	1	G	1	1	G	1	0	G	9
PB0_DATA42	1	R	2	1	V	2	1	G	2	1	G	2	nc	nc	nc
PB0_DATA43	1	R	3	1	V	3	1	G	3	1	G	3	nc	nc	nc
PB0_DATA44	1	R	4	1	V	4	1	G	4	1	G	4	1	R	8
PB0_DATA45	1	R	5	1	V	5	1	G	5	1	G	5	1	R	9
PB0_DATA46	1	R	6	1	V	6	1	G	6	1	G	6	nc	nc	nc

PB0_DATA47	1	R	7	1	V	7	1	G	7	1	G	7	nc	nc	nc
PB0_DATA48	nc	nc	nc	nc	nc	nc	1	B	0	1	R	0	1	B	0
PB0_DATA49	nc	nc	nc	nc	nc	nc	1	B	1	1	R	1	1	B	1
PB0_DATA50	nc	nc	nc	nc	nc	nc	1	B	2	1	R	2	1	B	2
PB0_DATA51	nc	nc	nc	nc	nc	nc	1	B	3	1	R	3	1	B	3
PB0_DATA52	nc	nc	nc	nc	nc	nc	1	B	4	1	R	4	1	B	4
PB0_DATA53	nc	nc	nc	nc	nc	nc	1	B	5	1	R	5	1	B	5
PB0_DATA54	nc	nc	nc	nc	nc	nc	1	B	6	1	R	6	1	B	6
PB0_DATA55	nc	nc	nc	nc	nc	nc	1	B	7	1	R	7	1	B	7
PB0_DATA56	nc	nc	nc	nc	nc	nc	1	A	0	1	A	0	1	B	8
PB0_DATA57	nc	nc	nc	nc	nc	nc	1	A	1	1	A	1	1	B	9
PB0_DATA58	nc	nc	nc	nc	nc	nc	1	A	2	1	A	2	nc	nc	nc
PB0_DATA59	nc	nc	nc	nc	nc	nc	1	A	3	1	A	3	nc	nc	nc
PB0_DATA60	nc	nc	nc	nc	nc	nc	1	A	4	1	A	4	1	G	8

Table 29: BGR8/YUV8_UYV/RGBA8/BGRA8/RGB10 Color Filters (Continued)

	BGR8			YUV8_UYV			RGBA8			BGRA8			RGB10		
	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA61	nc	nc	nc	nc	nc	nc	1	A	5	1	A	5	1	G	9
PB0_DATA62	nc	nc	nc	nc	nc	nc	1	A	6	1	A	6	nc	nc	nc
PB0_DATA63	nc	nc	nc	nc	nc	nc	1	A	7	1	A	7	nc	nc	nc
PB0_DATA64	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	1	G	0
PB0_DATA65	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	1	G	1
PB0_DATA66	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	1	G	2
PB0_DATA67	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	1	G	3
PB0_DATA68	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	1	G	4
PB0_DATA69	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	1	G	5
PB0_DATA70	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	1	G	6
PB0_DATA71	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	1	G	7
PB0_DATA72	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA73	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc

PB0_DATA74	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA75	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA76	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA77	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA78	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA79	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA80	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc

Table 29: BGR8/YUV8_UYV/RGBA8/BGRA8/RGB10 Color Filters (Continued)

	BGR8			YUV8_UYV			RGBA8			BGRA8			RGB10		
	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA81	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA82	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA83	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA84	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA85	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc

PB0_DATA86	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA87	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA88	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA89	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA90	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA91	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA92	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA93	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA94	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA95	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA96	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA97	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA98	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA99	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc

PB0_DATA100	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc

Table 29: BGR8/YUV8_UYV/RGBA8/BGRA8/RGB10 Color Filters (Continued)

	BGR8			YUV8_UYV			RGBA8			BGRA8			RGB10		
	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA101	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA102	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA103	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA104	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA105	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA106	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA107	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA108	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA109	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA110	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA111	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc

PB0_DATA112	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA113	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA114	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA115	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA116	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA117	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA118	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA119	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA120	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc

Table 29: BGR8/YUV8_UYV/RGBA8/BGRA8/RGB10 Color Filters (Continued)

	BGR8			YUV8_UYV			RGBA8			BGRA8			RGB10		
	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA121	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA122	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA123	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc

PB0_DATA124	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA125	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA126	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
PB0_DATA127	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc

Table 30: BGR10/RGB12/BGR12/YUV422_8_UYVY/YCbCrXXX_422_8_CbYCrY Color Filters

	BGR10			RGB12			BGR12			YUV422_8_UYVY a			YCbCrXXX_422_8_CbYCrY b c		
	Tap	Comp	Bit	Tap	Comp	Bit.	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA00	0	B	0	0	R	0	0	B	0	0	U/V	0	0	Cb/Cr	0
PB0_DATA01	0	B	1	0	R	1	0	B	1	0	U/V	1	0	Cb/Cr	1
PB0_DATA02	0	B	2	0	R	2	0	B	2	0	U/V	2	0	Cb/Cr	2
PB0_DATA03	0	B	3	0	R	3	0	B	3	0	U/V	3	0	Cb/Cr	3
PB0_DATA04	0	B	4	0	R	4	0	B	4	0	U/V	4	0	Cb/Cr	4
PB0_DATA05	0	B	5	0	R	5	0	B	5	0	U/V	5	0	Cb/Cr	5
PB0_DATA06	0	B	6	0	R	6	0	B	6	0	U/V	6	0	Cb/Cr	6

PB0_DATA07	0	B	7	0	R	7	0	B	7	0	U/V	7	0	Cb/Cr	7
PB0_DATA08	0	B	8	0	R	8	0	B	8	0	Y	0	0	Y	0
PB0_DATA09	0	B	9	0	R	9	0	B	9	0	Y	1	0	Y	1
PB0_DATA10	nc	nc	nc	0	R	10	0	B	10	0	Y	2	0	Y	2
PB0_DATA11	nc	nc	nc	0	R	11	0	B	11	0	Y	3	0	Y	3
PB0_DATA12	0	R	8	0	B	8	0	R	8	0	Y	4	0	Y	4
PB0_DATA13	0	R	9	0	B	9	0	R	9	0	Y	5	0	Y	5
PB0_DATA14	nc	nc	nc	0	B	10	0	R	10	0	Y	6	0	Y	6
PB0_DATA15	nc	nc	nc	0	B	11	0	R	11	0	Y	7	0	Y	7
PB0_DATA16	0	R	0	0	B	0	0	R	0	1	V	0	1	Cr	0
PB0_DATA17	0	R	1	0	B	1	0	R	1	1	V	1	1	Cr	1
PB0_DATA18	0	R	2	0	B	2	0	R	2	1	V	2	1	Cr	2
PB0_DATA19	0	R	3	0	B	3	0	R	3	1	V	3	1	Cr	3
PB0_DATA20	0	R	4	0	B	4	0	R	4	1	V	4	1	Cr	4

Table 30: BGR10/RGB12/BGR12/YUV422_8_UYVY/YCbCrXXX_422_8_CbYCrY Color Filters (Continued)

	BGR10			RGB12			BGR12			YUV422_8_UYVY a			YCbCrXXX_ 422_8_CbYCrY b c		
	Tap	Comp	Bit	Tap	Comp	Bit.	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA21	0	R	5	0	B	5	0	R	5	1	V	5	1	Cr	5
PB0_DATA22	0	R	6	0	B	6	0	R	6	1	V	6	1	Cr	6
PB0_DATA23	0	R	7	0	B	7	0	R	7	1	V	7	1	Cr	7
PB0_DATA24	1	B	0	1	R	0	1	B	0	1	Y	0	1	Y	0
PB0_DATA25	1	B	1	1	R	1	1	B	1	1	Y	1	1	Y	1
PB0_DATA26	1	B	2	1	R	2	1	B	2	1	Y	2	1	Y	2
PB0_DATA27	1	B	3	1	R	3	1	B	3	1	Y	3	1	Y	3
PB0_DATA28	1	B	4	1	R	4	1	B	4	1	Y	4	1	Y	4
PB0_DATA29	1	B	5	1	R	5	1	B	5	1	Y	5	1	Y	5
PB0_DATA30	1	B	6	1	R	6	1	B	6	1	Y	6	1	Y	6
PB0_DATA31	1	B	7	1	R	7	1	B	7	1	Y	7	1	Y	7
PB0_DATA32	0	G	0	0	G	0	0	G	0	2	U	0	2	Cb	0

PB0_DATA33	0	G	1	0	G	1	0	G	1	2	U	1	2	Cb	1
PB0_DATA34	0	G	2	0	G	2	0	G	2	2	U	2	2	Cb	2
PB0_DATA35	0	G	3	0	G	3	0	G	3	2	U	3	2	Cb	3
PB0_DATA36	0	G	4	0	G	4	0	G	4	2	U	4	2	Cb	4
PB0_DATA37	0	G	5	0	G	5	0	G	5	2	U	5	2	Cb	5
PB0_DATA38	0	G	6	0	G	6	0	G	6	2	U	6	2	Cb	6
PB0_DATA39	0	G	7	0	G	7	0	G	7	2	U	7	2	Cb	7
PB0_DATA40	0	G	8	0	G	8	0	G	8	2	Y	0	2	Y	0

Table 30: BGR10/RGB12/BGR12/YUV422_8_UYVY/YCbCrXXX_422_8_CbYCrY Color Filters (Continued)

	BGR10			RGB12			BGR12			YUV422_8_UYVY a			YCbCrXXX_ 422_8_CbYCrY bc		
	Tap	Comp	Bit	Tap	Comp	Bit.	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA41	0	G	9	0	G	9	0	G	9	2	Y	1	2	Y	1
PB0_DATA42	nc	nc	nc	0	G	10	0	G	10	2	Y	2	2	Y	2
PB0_DATA43	nc	nc	nc	0	G	11	0	G	11	2	Y	3	2	Y	3

PB0_DATA44	1	B	8	1	R	8	1	B	8	2	Y	4	2	Y	4
PB0_DATA45	1	B	9	1	R	9	1	B	9	2	Y	5	2	Y	5
PB0_DATA46	nc	nc	nc	1	R	10	1	B	10	2	Y	6	2	Y	6
PB0_DATA47	nc	nc	nc	1	R	11	1	B	11	2	Y	7	2	Y	7
PB0_DATA48	1	R	0	1	B	0	1	R	0	3	V	0	3	Cr	0
PB0_DATA49	1	R	1	1	B	1	1	R	1	3	V	1	3	Cr	1
PB0_DATA50	1	R	2	1	B	2	1	R	2	3	V	2	3	Cr	2
PB0_DATA51	1	R	3	1	B	3	1	R	3	3	V	3	3	Cr	3
PB0_DATA52	1	R	4	1	B	4	1	R	4	3	V	4	3	Cr	4
PB0_DATA53	1	R	5	1	B	5	1	R	5	3	V	5	3	Cr	5
PB0_DATA54	1	R	6	1	B	6	1	R	6	3	V	6	3	Cr	6
PB0_DATA55	1	R	7	1	B	7	1	R	7	3	V	7	3	Cr	7
PB0_DATA56	1	R	8	1	B	8	1	R	8	3	Y	0	3	Y	0
PB0_DATA57	1	R	9	1	B	9	1	R	9	3	Y	1	3	Y	1

PB0_DATA58	nc	nc	nc	1	B	10	1	R	10	3	Y	2	3	Y	2
PB0_DATA59	nc	nc	nc	1	B	11	1	R	11	3	Y	3	3	Y	3
PB0_DATA60	1	G	8	1	G	8	1	G	8	3	Y	4	3	Y	4

Table 30: BGR10/RGB12/BGR12/YUV422_8_UYVY/YCbCrXXX_422_8_CbYCrY Color Filters (Continued)

	BGR10			RGB12			BGR12			YUV422_8_UYVY a			YCbCrXXX_422_8_CbYCrY b c		
	Tap	Comp	Bit	Tap	Comp	Bit.	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA61	1	G	9	1	G	9	1	G	9	3	Y	5	3	Y	5
PB0_DATA62	nc	nc	nc	1	G	10	1	G	10	3	Y	6	3	Y	6
PB0_DATA63	nc	nc	nc	1	G	11	1	G	11	3	Y	7	3	Y	7
PB0_DATA64	1	G	0	1	G	0	1	G	0	4	U	0	4	Cb	0
PB0_DATA65	1	G	1	1	G	1	1	G	1	4	U	1	4	Cb	1
PB0_DATA66	1	G	2	1	G	2	1	G	2	4	U	2	4	Cb	2
PB0_DATA67	1	G	3	1	G	3	1	G	3	4	U	3	4	Cb	3
PB0_DATA68	1	G	4	1	G	4	1	G	4	4	U	4	4	Cb	4

PB0_DATA69	1	G	5	1	G	5	1	G	5	4	U	5	4	Cb	5
PB0_DATA70	1	G	6	1	G	6	1	G	6	4	U	6	4	Cb	6
PB0_DATA71	1	G	7	1	G	7	1	G	7	4	U	7	4	Cb	7
PB0_DATA72	nc	nc	nc	nc	nc	nc	nc	nc	nc	4	Y	0	4	Y	0
PB0_DATA73	nc	nc	nc	nc	nc	nc	nc	nc	nc	4	Y	1	4	Y	1
PB0_DATA74	nc	nc	nc	nc	nc	nc	nc	nc	nc	4	Y	2	4	Y	2
PB0_DATA75	nc	nc	nc	nc	nc	nc	nc	nc	nc	4	Y	3	4	Y	3
PB0_DATA76	nc	nc	nc	nc	nc	nc	nc	nc	nc	4	Y	4	4	Y	4
PB0_DATA77	nc	nc	nc	nc	nc	nc	nc	nc	nc	4	Y	5	4	Y	5
PB0_DATA78	nc	nc	nc	nc	nc	nc	nc	nc	nc	4	Y	6	4	Y	6
PB0_DATA79	nc	nc	nc	nc	nc	nc	nc	nc	nc	4	Y	7	4	Y	7
PB0_DATA80	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	V	0	5	Cr	0

Table 30: BGR10/RGB12/BGR12/YUV422_8_UYVY/YCbCrXXX_422_8_CbYCrY Color Filters (Continued)

	BGR10	RGB12	BGR12	YUV422_8_UYVY a	YCbCrXXX_ 422_8_CbYCrY b c

	Tap	Comp	Bit	Tap	Comp	Bit.	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA81	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	V	1	5	Cr	1
PB0_DATA82	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	V	2	5	Cr	2
PB0_DATA83	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	V	3	5	Cr	3
PB0_DATA84	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	V	4	5	Cr	4
PB0_DATA85	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	V	5	5	Cr	5
PB0_DATA86	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	V	6	5	Cr	6
PB0_DATA87	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	V	7	5	Cr	7
PB0_DATA88	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	Y	0	5	Y	0
PB0_DATA89	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	Y	1	5	Y	1
PB0_DATA90	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	Y	2	5	Y	2
PB0_DATA91	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	Y	3	5	Y	3
PB0_DATA92	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	Y	4	5	Y	4
PB0_DATA93	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	Y	5	5	Y	5

PB0_DATA94	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	Y	6	5	Y	6
PB0_DATA95	nc	nc	nc	nc	nc	nc	nc	nc	nc	5	Y	7	5	Y	7
PB0_DATA96	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	U	0	6	Cb	0
PB0_DATA97	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	U	1	6	Cb	1
PB0_DATA98	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	U	2	6	Cb	2
PB0_DATA99	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	U	3	6	Cb	3
PB0_DATA100	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	U	4	6	Cb	4

Table 30: BGR10/RGB12/BGR12/YUV422_8_UYVY/YCbCrXXX_422_8_CbYCrY Color Filters (Continued)

	BGR10			RGB12			BGR12			YUV422_8_UYVY [a]			YCbCrXXX_422_8_CbYCrY [b] [c]		
	Tap	Comp	Bit	Tap	Comp	Bit.	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA101	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	U	5	6	Cb	5
PB0_DATA102	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	U	6	6	Cb	6
PB0_DATA103	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	U	7	6	Cb	7
PB0_DATA104	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	Y	0	6	Y	0

PB0_DATA105	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	Y	1	6	Y	1
PB0_DATA106	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	Y	2	6	Y	2
PB0_DATA107	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	Y	3	6	Y	3
PB0_DATA108	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	Y	4	6	Y	4
PB0_DATA109	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	Y	5	6	Y	5
PB0_DATA110	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	Y	6	6	Y	6
PB0_DATA111	nc	nc	nc	nc	nc	nc	nc	nc	nc	6	Y	7	6	Y	7
PB0_DATA112	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	V	0	7	Cr	0
PB0_DATA113	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	V	1	7	Cr	1
PB0_DATA114	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	V	2	7	Cr	2
PB0_DATA115	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	V	3	7	Cr	3
PB0_DATA116	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	V	4	7	Cr	4
PB0_DATA117	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	V	5	7	Cr	5
PB0_DATA118	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	V	6	7	Cr	6

PB0_DATA119	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	V	7	7	Cr	7
PB0_DATA120	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	Y	0	7	Y	0

Table 30: BGR10/RGB12/BGR12/YUV422_8_UYVY/YCbCrXXX_422_8_CbYCrY Color Filters (Continued)

	BGR10			RGB12			BGR12			YUV422_8_UYVY a			YCbCrXXX_422_8_CbYCrY b c		
	Tap	Comp	Bit	Tap	Comp	Bit.	Tap	Comp	Bit	Tap	Comp	Bit	Tap	Comp	Bit
PB0_DATA121	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	Y	1	7	Y	1
PB0_DATA122	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	Y	2	7	Y	2
PB0_DATA123	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	Y	3	7	Y	3
PB0_DATA124	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	Y	4	7	Y	4
PB0_DATA125	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	Y	5	7	Y	5
PB0_DATA126	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	Y	6	7	Y	6
PB0_DATA127	nc	nc	nc	nc	nc	nc	nc	nc	nc	7	Y	7	7	Y	7

a When only one tap is used for YUV422_8_UYVY, Tap 0 alternate between U and V. When more than one tap are used, Tap 0 is component U.

b When only one tap is used for YCbCrXXX_422_8_CbYCrY, Tap 0 alternate between Cb and Cr. When more than one tap are used, Tap 0 is component Cb.

c YCbCrXXX_422_8_CbYCrY is for YCbCr601_422_8_CbYCrY and YCbCr709_422_8_CbYCrY.

7 Signal Handling

The NTx-Deca includes a programmable logic controller (PLC) that lets you control external machines and react to inputs. By controlling your system using the PLC, you can make functional changes, adjust timing, or add features without having to add new hardware.

7.1 PLC Programming Signals

For an introduction to the PLC and for detailed information about how PLC signals are handled, see the *iPORT Advanced Features User Guide*, available on the Pleora Support Center at www.pleora.com.

The following table lists the PLC input and output programming signals that are specific to the embedded video interface, and indicates the pins on which they are available.

Table 31: PLC Signal Usage

Signal name	PLC equation usage	Associated pin
Pb0Fval	Input	Pin 24 and 26 on the J3 40-pin user circuitry connector, LVDS0_DATA6_P/N, serialized bit FVAL.
Pb0Lval	Input	Pin 24 and 26 on the J3 40-pin user circuitry connector, LVDS0_DATA6_P/N, serialized bit LVAL.
Pb0Dval	Input	Pin 24 and 26 on the J3 40-pin user circuitry connector, LVDS0_DATA6_P/N, serialized bit DVAL.
Pb0Spare	Input	Pin 24 and 26 on the J3 40-pin user circuitry connector, LVDS0_DATA6_P/N, serialized bit SPR. **Note**: When chunk data is in use, this signal is Metadata Valid (MVAL). For more information about chunk data and MVAL, see the iPORT Advanced Features User Guide, available on the Pleora Support Center at Home - Pleora Technologies[1] .
GpioIn0	Input	Pin 31 on the J1 40-pin user circuitry connector, FPGA_GPIO_IN0
GpioIn1	Input	Pin 35 on the J1 40-pin user circuitry connector, FPGA_GPIO_IN1

1. http://www.pleora.com/

GpioIn2	Input	Pin 22 on the J1 40-pin user circuitry connector, FPGA_GPIO_IN2
GpioIn3	Input	Pin 29 on the J1 40-pin user circuitry connector, FPGA_GPIO_IN3
BufferWM0	Input	No associated pin
Grb0AcqActive	Input	No associated pin
PlcCtrl0	Input	No associated pin
PlcCtrl1	Input	No associated pin
PlcCtrl2	Input	No associated pin
PlcCtrl3	Input	No associated pin
Pb0CC1	Input, output	Pin 35 on the J3 40-pin user circuitry connector, PB0_CTRL_OUT1
Pb0CC2	Input, output	Pin 37 on the J3 40-pin user circuitry connector, PB0_CTRL_OUT2
Pb0CC3	Input, output	Pin 36 on the J1 40-pin user circuitry connector, BULK_CS1_PCO3
GpioOut0	Input, output	Pin 32 on the J1 40-pin user circuitry connector, FPGA_GPIO_OUT0
GpioOut1	Input, output	Pin 30 on the J1 40-pin user circuitry connector, FPGA_GPIO_OUT1

Table 31: PLC Signal Usage (Continued)

Signal name	PLC equation usage	Associated pin
PlcFval0	Input, output	No associated pin
PlcLval0	Input, output	No associated pin
PlcMval0	Input, output	No associated pin

PlcTrig0	Input, output	No associated pin
PlcTimestampCtrl	Input, output	No associated pin
Timer0Trig	Input, output	No associated pin
Timer0Out	Input	No associated pin
Timer1Trig	Input, output	No associated pin
Timer1Out	Input	No associated pin
Counter0Reset	Input, output	No associated pin
Counter0Inc	Input, output	No associated pin
Counter0Dec	Input, output	No associated pin
Counter0Eq	Input	No associated pin
Counter0Gt	Input	No associated pin
Counter1Reset	Input, output	No associated pin
Counter1Inc	Input, output	No associated pin
Counter1Dec	Input, output	No associated pin
Counter1Eq	Input	No associated pin
Counter1Gt	Input	No associated pin

Table 31: PLC Signal Usage (Continued)

Signal name	PLC equation usage	Associated pin
Rescaler0In	Input, output	No associated pin
Rescaler0Out	Input	No associated pin

Delayer0In	Input, output	No associated pin
Delayer0Out	Input	No associated pin
Event0	Input, output	No associated pin
Event1	Input, output	No associated pin
Event2	Input, output	No associated pin
Event3	Input, output	No associated pin
ActionTrig0	Input	No associated pin
ActionTrig1	Input	No associated pin

8 Installing the eBUS SDK

This chapter describes how to install the eBUS SDK, and also provides information about installing the required driver.

Before you can configure and control your NTx-Deca, you must install the eBUS SDK.

8.1 Installing the eBUS SDK

You can install the Pleora Technologies eBUS SDK on your computer to configure and control your NTx-Deca.

The eBUS SDK contains an extensive library of sample applications, with source code, to create working applications for device configuration and control, image and data acquisition, and image display and diagnostics.

It is possible for you to configure the NTx-Deca and GigE Vision compliant video sources using other GenICam compliant software; however, this guide provides you with the instructions you need to use the Pleora eBUS Player application.

8.2 Installing the Driver

The eBUS SDK includes a GigE Vision driver that enhances existing general-purpose drivers shipped with NICs, increases image acquisition throughput and performance, decreases latency and jitter, and minimizes CPU utilization.

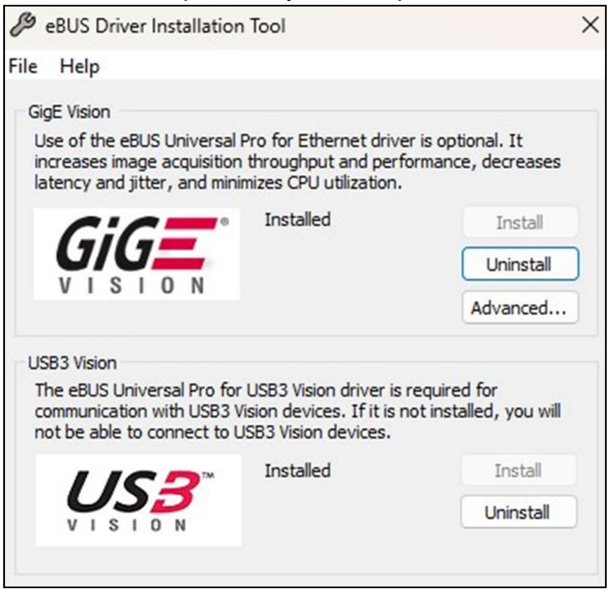
The USB3 Vision driver, which is available during the installation of the eBUS SDK, is for use with USB3 Vision compliant devices.

The drivers are selected for installation by default during the eBUS SDK installation process. If you choose not to install the drivers (or want to uninstall either driver), you can use the eBUS Driver Installation Tool.

To use the eBUS Driver Installation Tool

1. Click Start > All apps > Pleora Technologies Inc > eBUS SDK > eBUS Driver Installation Tool.
2. Under **GigE Vision**, click **Install** or **Uninstall**.
   After a moment, the driver status changes. If you are installing a driver, the driver is installed across

all network adapters on your computer.



3. Close the eBUS Driver Installation Tool.
   You may be required to restart your computer.

> To see the versions of the installed drivers, click Help > About.

9 Configuring Your Computer’s NIC for use with the NTx-Deca

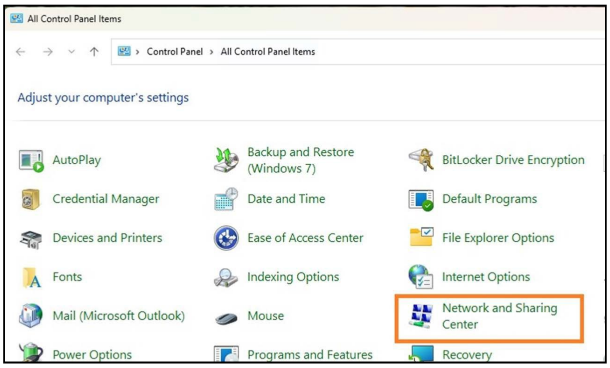
This chapter explains how to configure your computer’s NIC for communication with the NTx-Deca.

For optimal performance, we recommend that you enable jumbo packets (also known as jumbo frames) and set the receive descriptors to the maximum available value.

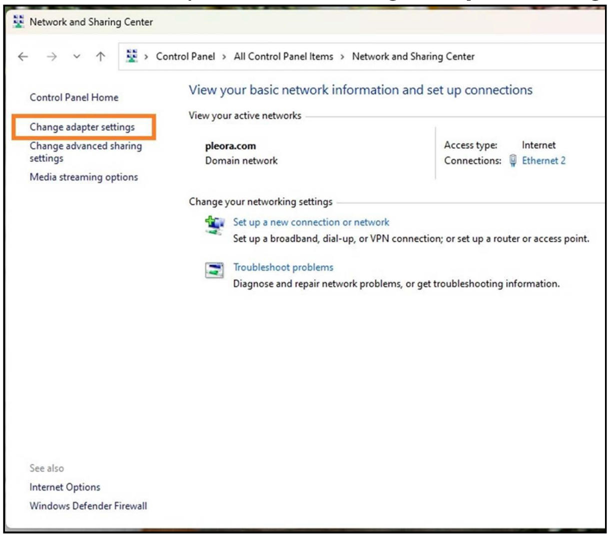
> The instructions in this section are based on the Windows 11 operating system. The steps may vary depending on your computer’s operating system.

To configure the NIC for optimal performance

1. In the Windows Control Panel, click **Network and Sharing Center**.

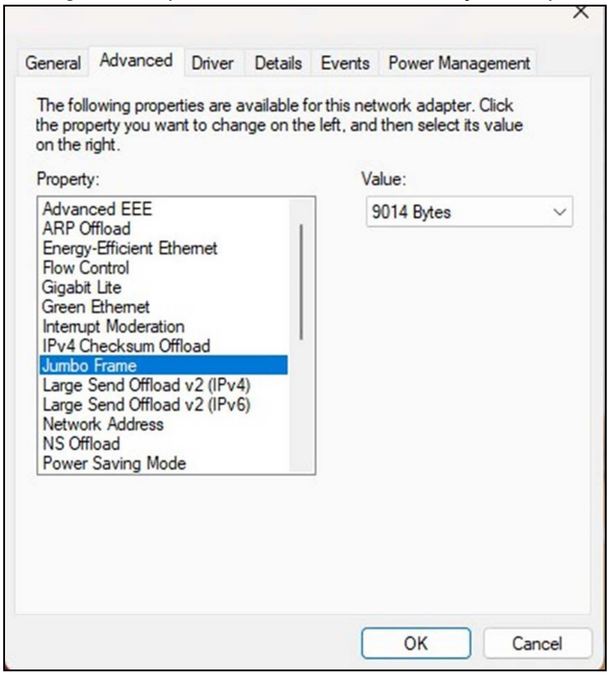


2. In the left-hand panel, click **Change adapter settings**.



3. Configure the NIC for jumbo packets (often referred to as jumbo frames) and set the NIC’s **Receive Buffers (Receive Descriptors)** to the maximum available Using jumbo packets allows you to increase system performance. However, you must ensure your NIC and 10GBASE-T switch (if applicable) support jumbo packets.

To complete this task, right-click the NIC and click **Properties**. Then, click **Configure**. The exact configuration procedure, as well as the jumbo packet size limit, depends on the NIC.



4. Close the open dialog boxes to apply the changes and close the Control Panel.

10 Connecting to the NTx-Deca and Configuring General Settings

After you have set up the physical connections to the NTx-Deca, you can start the eBUS Player application to configure image settings to ensure images are received and displayed properly. You can also configure the buffer options to reduce the likelihood of lost packets.

eBUS Player is documented in more detail in the *eBUS Player User Guide*. This guide only provides you with high-level eBUS Player instructions to help you set up your device and to start streaming video. The *eBUS Player User Guide* is available on the Pleora Support Center (https://supportcenter.pleora.com/).

10.1 Confirming Image Streaming

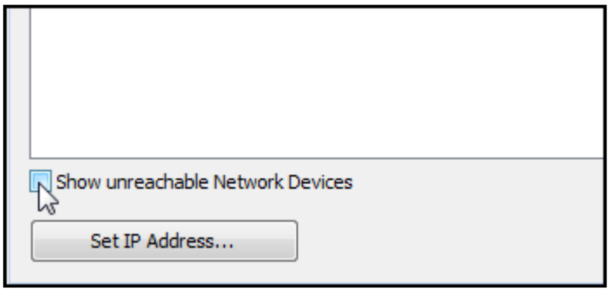
The embedded video interface can communicate with your computer using either a direct connection or by connecting to a GigE or 10GBASE-T switch.

To connect the cables and apply power

- Connect the NTx-Deca to the RJ-45 Ethernet connector on your computer's NIC or a GigE or 10GBASE-T switch. Then, apply power.

To start eBUS Player and connect to a device

1. Start eBUS Player from the Windows **Start** menu.
2. Click **Select/Connect**.
   If the NTx-Deca does not appear in the list, click the **Show unreachable Network Devices** check box to show all devices.



3. In the **Device Selection** dialog box, click the embedded video interface.

If the IP address is not compatible with your NIC, a warning ( ) appears in the Device Selection dialog box. Provide the device with an IP address, as outlined in "Providing the NTx-Deca with an IP Address".

4. Click **OK**.
   eBUS Player is now connected to the embedded video interface.

To confirm image streaming

1. Click **Play** to stream live images or the test pattern.
   For information about using the test pattern, see “To turn the test pattern on or off”
2. After you confirm that images are streaming, click **Stop**.

If images do not stream, see the tips provided in “System Troubleshooting”.

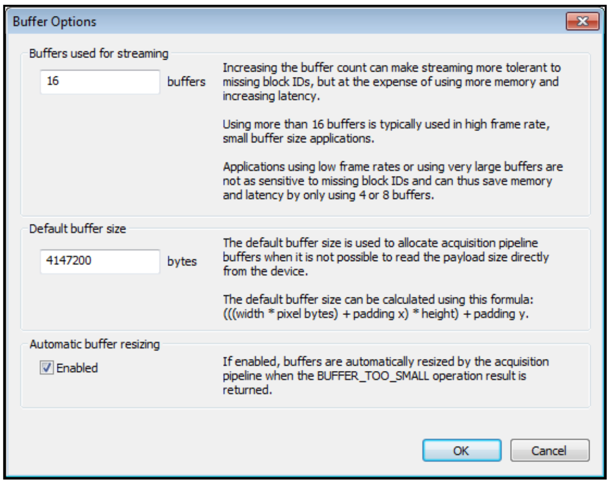
10.2 Configuring the Buffers

You can increase the buffer count using eBUS Player to make streaming more robust. A high number of buffers are needed in high frame rate applications, while a small number of buffers are needed for lower frame rates. Latency increases as the number of buffers increases.

To configure the buffers

1. Start eBUS Player and connect to the embedded video interface.
   For more information, see “To start eBUS Player and connect to a device”
2. Click **Tools** > **Buffer Options**.
3. Click the buffer option that suits your requirements.
4. Click **OK**.

Default size for streaming is 16 buffers.



10.3 Providing the NTx-Deca with an IP Address

The NTx-Deca requires an IP address to communicate on a video network. This address must be on the same subnet as the computer that is performing the configuration and receiving the image stream.

To provide the NTx-Deca with an IP address

1. Start eBUS Player.
2. Click **Select/Connect**.
3. Click the NTx-Deca.
4. Click **Set IP Address**.
5. Provide the embedded video interface with a compatible IP address and subnet You can optionally provide a default gateway.
   Note that this information is temporary and is reset when you power down the device. To set an IP address that is used permanently, see the next procedure in this guide.

   > ⚠ If you are using a unicast network configuration, the management entity/data receiver and the embedded video interface must be on the same subnet. The unicast network configuration is outlined in “Unicast Network Configuration”

6. Click **OK** to close the **Set IP Address** dialog box.
7. Click **OK** to close the **Device Selection** dialog box and connect to the device.

10.3.1 Configuring an Automatic/Persistent IP Address

The Device Control dialog box allows you to configure a persistent IP address for the NTx-Deca. Alternatively, the embedded video interface can be configured to automatically obtain an IP address using Dynamic Host Configuration Protocol (DHCP) or Link Local Addressing (LLA). The embedded video interface uses its persistent IP address first, but if this option is set to **False**, it can be configured to attempt to obtain an address from a DHCP server. If this fails, it will use LLA to find an available IP address. LLA cannot be disabled and is always set to **True**.

> ✅ The device can use the persistent IP address each time it is powered up as long as the IP address is valid and there are no IP address conflicts

To configure a persistent IP address

1. Start eBUS Player and connect to the NTx-Deca.
   For more information, see “To start eBUS Player and connect to a device”
2. Under **Parameters and Controls**, click **Device control**.
3. Under **TransportLayerControl**, set the **GevCurrentIPConfigurationPersistentIP** feature to **True**.

4. Set the **GevPersistentIPAddress** feature to a valid IP address in the **GevPersistentIPAddress** field.
5. Set the **GevPersistentSubnetMask** feature to a valid subnet mask address.
6. Optionally, enter a valid default gateway in the **GevPersistentDefaultGateway** field.
7. Close the **Device Control** dialog box.
8. Power cycle the embedded video interface.

To automatically configure an IP address

1. Start eBUS Player and connect to the NTx-Deca.
   For more information, see "To start eBUS Player and connect to a device"
2. Under **Parameters and Controls**, click **Device control**.
   Under **TransportLayerControl**, set the **GevCurrentIPConfigurationPersistentIP** feature to **False**.
3. Set the **GevCurrentIPConfigurationLLA** and/or **GevCurrentIPConfigurationDHCP** values to **True**, depending on the type of automatic addressing you require.
4. Close the **Device Control** dialog box.
5. Power cycle the embedded video interface.

10.4 Configuring the NTx-Deca Image Settings

You can configure the NTx-Deca image settings, which provide the embedded video interface with information about the image coming from the camera. These settings allow the images to appear correctly.

The image settings are located under **ImageFormatControl** in the **Device Control** dialog box.

> Changes that you make to the NTx-Deca are not persisted across power cycles, unless you use the UserSetSave feature. For information about saving settings to the NTx-Deca's flash memory, see the *eBUS Player User Guide*, available on the Pleora Support Center.

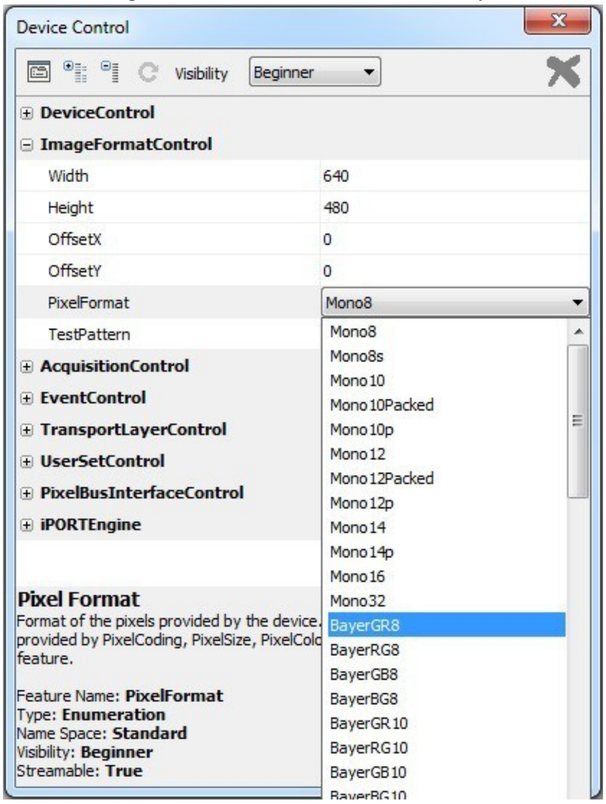
To turn the test pattern on or off

1. Start eBUS Player and connect to the embedded video interface.
   For more information, see "To start eBUS Player and connect to a device"
2. Under **Parameters and Controls**, click **Device control**.
3. Under **ImageFormatControl**, click find the TestPattern feature and select NOTE: to disable the TestPattern and stream data over the sensor interface, set TestPattern = Off..
4. Close the **Device Control** dialog box.

To reduce the amount of bandwidth that is used when transmitting the test pattern, increase the OffsetX and OffsetY values. Increasing OffsetX reduces the bandwidth by a factor of two. Increasing both OffsetX and OffsetY reduces the bandwidth by a factor of 4. An OffsetX and OffsetY of 0 will require the most bandwidth.

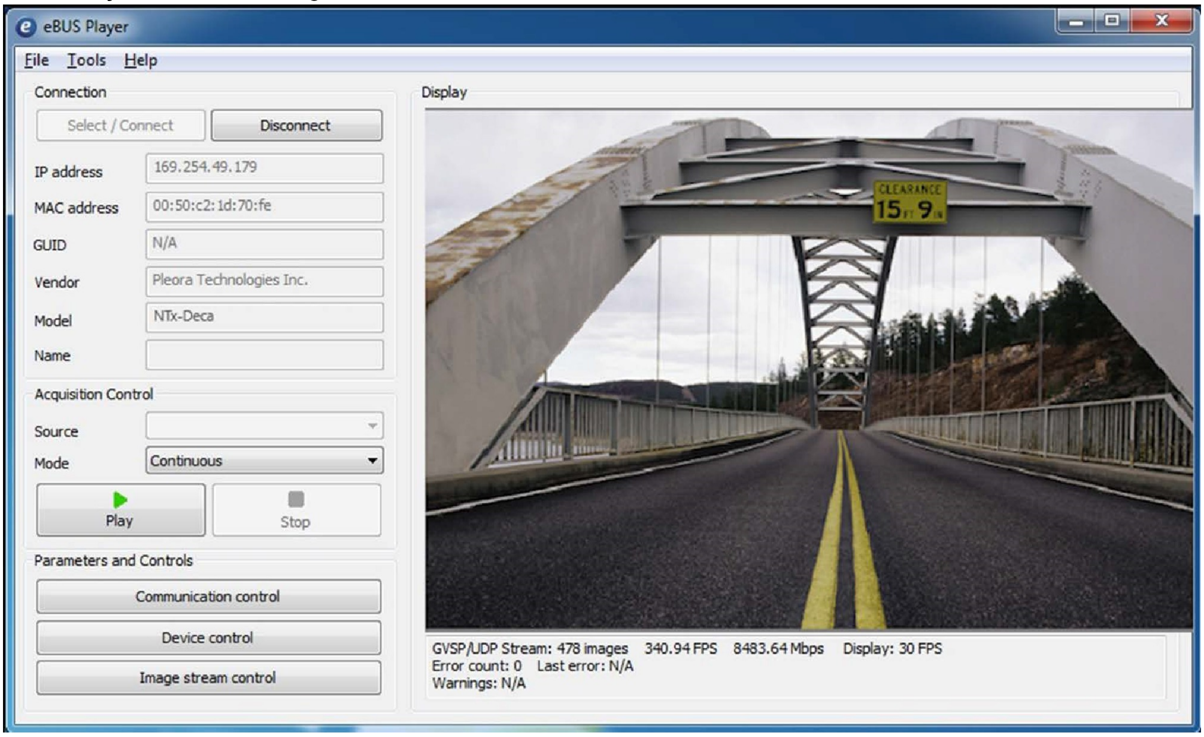
To change the pixel format

1. Start eBUS Player and connect to the embedded video interface.
   For more information, see "To start eBUS Player and connect to a device"
2. If images are streaming, click the **Stop** button.
3. Under **Parameters and Controls**, click **Device control**.
4. Under **ImageFormatControl**, choose the pixel format that matches your camera's configuration.



5. Close the **Device Control** dialog box.

6. Click **Play** to see the changes.

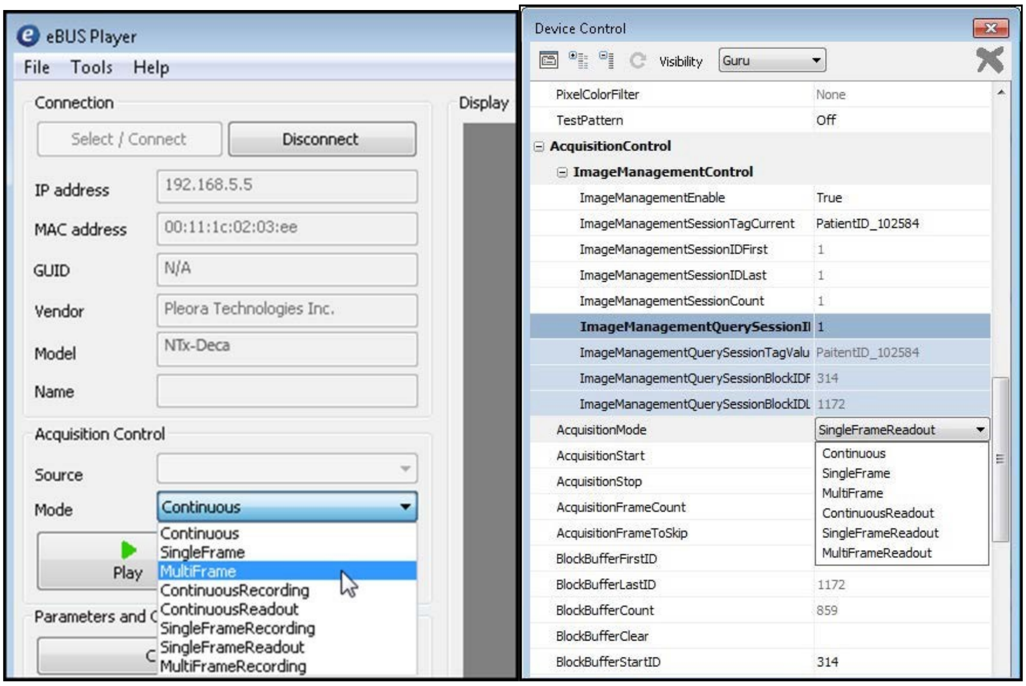


To configure the image width and height

1. Start eBUS Player and connect to the embedded video interface.
   For more information, see "To start eBUS Player and connect to a device"
2. If images are streaming, click the **Stop** button.
3. Under **Parameters and Controls**, click **Device control**.
4. Under **ImageFormatControl**, change the **Width** and **Height** to suit your camera.
5. Close the **Device Control** dialog box.

10.5 Specifying How Images are Acquired

Continuous, SingleFrame, and MultiFrame modes are usually standard for embedded video interfaces. Acquisition starts when the Play button is pressed (the AcquisitionStart command is executed).



10.5.1 Continuous Mode

This mode allows you to acquire images continuously and is the default mode for most embedded video interfaces.

10.5.2 Multiframe Mode

This mode allows you to acquire a fixed number of images. To configure the number of images, set the embedded video interface's **AcquisitionControl** > **AcquisitionFrameCount** feature.

You can set the **AcquisitionControl** > **AcquisitionFrameCount** feature in the **Device Control** dialog box.

10.5.3 SingleFrame Mode

This mode allows you to acquire one image at a time.

10.6 Recording and Retrieving Images in the Onboard Memory

In addition to the standard acquisition modes listed in the previous section, the embedded video interface also has recording and readout modes.

> When using the image management feature, the readout modes operate in a slightly different manner. This section describes how these modes operate when AcquisitionControl > ImageManagementEnable feature is set to False. For information about using the readout modes when image management is enabled, see "Image Management Feature"

The **recording** acquisition modes allow you to capture images from a camera and store them in the embedded video interface's onboard memory.

The **readout** acquisition modes allow images to be retrieved from the device's memory at a slower rate, ensuring images are not lost.

These modes are helpful when you are working with a camera that transmits images at a rate that exceeds the connection between the embedded video interface and the computer, resulting in dropped images. By using the recording and readout modes in this example, you can capture and stream images from the camera without losing any images (as long as there is space in the onboard memory).

The recording acquisition modes support back-to-back recording, which allows you to click the **Stop** and

Play buttons multiple consecutive times without clearing the onboard memory.

Acquisition starts when the **Play** button is pressed (the **AcquisitionStart** command is executed) and when one of the recording modes is selected.

Images can be stored in the onboard memory as long as there is space or until there are 4096 images in memory. For information about calculating how many images you can store, see "Calculating How Many Images Can be Stored in Onboard Memory"

10.6.1 Continuous Recording Mode

With this mode, images are acquired continuously and are stored in the device's onboard memory until the memory is full (or 4096 images are stored in onboard memory). When this limit is reached, the NTx-Deca stops acquiring new images from the camera.

We recommend that you observe **AcquisitionControl** > **BlockBufferCount** in eBUS Player's **Device Control** dialog box (**Expert** or **Guru** visibility level is required). When the value for this feature stops increasing, the memory is full. For information about the actions that clear the images from onboard memory, see "Understanding When Images are Removed from the Onboard Memory"

10.6.2 Continuous Readout Mode

With this mode, images are continuously read (and removed) from the device's onboard memory. The readout begins at the first image in memory. To see the number of images stored in onboard memory, see **AcquisitionControl** > **BlockBufferCount** in eBUS Player's **Device Control** dialog box (**Expert** or **Guru** visibility level is required).

Readout continues until the **Stop** button is pressed (**AcquisitionStop** command is executed) or until the last image has been sent by the device (**BlockBufferCount** will be **0**).

10.6.3 Multi Frame Recording Mode

With this mode, a fixed number of images are stored in the device's onboard memory. To configure the number of images, set the **AcquisitionControl** > **AcquisitionFrameCount** feature in eBUS Player's **Device Control** dialog box. Images can be read out from memory using **Continuous Readout mode**.

A maximum of 255 images can be acquired at one time in Multi Frame Recording mode.

To determine how many images can be stored in memory, see "Calculating How Many Images Can be Stored in Onboard Memory".

If **AcquisitionControl** > **AcquisitionFrameCount** is set to a value that exceeds the amount of available memory, the embedded video interface stops acquiring new images when the onboard memory is full (or 4096 images are stored in onboard memory).

BlockBufferCount shows the number of images currently in memory. In **Multi Frame Recording mode**, this number is cumulative: If the memory is empty and you acquire an image, **BlockBufferCount** will match the **AcquisitionFrameCount**. If you stop and restart recording, **BlockBufferCount** will increment (to a maximum of 4096 images, depending on the image size) and will no longer match the **AcquisitionFrameCount**.

10.6.4 Single Frame Recording Mode

With this mode, a single image is saved in the embedded video interface's onboard memory after each **AcquisitionStart** command.

10.6.5 Single Frame Readout Mode

With this mode, only a single image is read out from the device's memory at a slower rate, ensuring images are not lost. This mode is helpful when you are working with a camera that transmits images at a rate that exceeds the connection between the embedded video interface and the computer, resulting in dropped images.

10.6.6 Understanding When Recorded Images are Removed from the Onboard Memory.

This section is for Recording and Readout when ImageManagementEnabled is set to False.

The following actions remove the images from the NTx-Deca's onboard memory:

- Images read by any Readout mode
- Power cycling the device, which clears all images from the onboard memory.
- Making any of the following **AcquisitionMode** changes and then clicking the **Play** button (**AcquisitionStart** command), all unread images will be removed.
  From any Recording or Readout mode to any Streaming mode
  From any Readout mode to any Recording mode

10.6.7 Calculating How Many Images Can be Stored in Onboard Memory

First, take note of the **PayloadSize**, which appears under **TransportLayerControl** in eBUS Player's **Device Control** dialog box. **Expert** or **Guru** visibility level is required to access this feature.

The **PayloadSize** is automatically calculated by the device based on the selected image settings, which include **Width**, **Height**, **OffsetX**, **OffsetY**, **PixelSize**, any chunk data, as well as any padding that has to be added to the image payload.

For example, for a device configured to use Mono8 with images that are 1920 x 1080, the **PayloadSize** is equal to 2 073 600 bytes per image or about 1.978 MB (2 073 600 / 1 048 576).

After determining **PayloadSize**, you can use the following equation to determine the number of images that can be saved in onboard memory:

Available onboard memory MB / PayloadSize MB = Number of images that can be saved

Using our example, the equation is:

1007.50 MB / 1.978 MB = 509 images

10.7 Image Management Feature

In some systems you may be interested in keeping track of images that were transmitted during a particular acquisition session, in case you need to retransmit them to a receiving computer. This can be useful in systems where you want images to be available in the event that the receiving computer experiences a malfunction or a loss of power or when the embedded video interface experiences a loss of power.

The image management feature lets you specify a unique session tag before you start acquiring images, which indicates that the images belong to the same session. It also provides contextual information that will help you identify the session so you can retrieve it from the embedded video interface's memory.

As you continue to start new sessions (which requires that you specify a new unique session tag to mark the beginning of a new session), a directory structure forms within the onboard memory and you will have a selection of acquisition sessions that you can retrieve.

Note that the sessions and associated images are stored in the device's onboard memory and are not copied to non-volatile storage. A loss of power on the embedded video interface will result in the loss of the directory and all images.

To keep track of images captured during a session, complete the following tasks, which are described in detail later in this section:

- Enable image management.
- Specify an alphanumeric session tag that will be used to identify the All of the images with this tag are considered to be a part of the same session. When you begin a different session, you can use a different session tag to start a new session.
- Choose an acquisition mode (Continuous, SingleFrame, or MultiFrame) and start image acquisition.
- After streaming starts, the group of images are tagged with an automatically generated session ID number (which is associated with the user-defined session tag).
  Note: When there is no more space to store images or there are 4096 images in memory, the oldest images will start being overwritten with new ones.
- Retrieve the images by selecting a readout acquisition mode and starting a You can retrieve the first or last image in the session, or an image with a particular block ID.

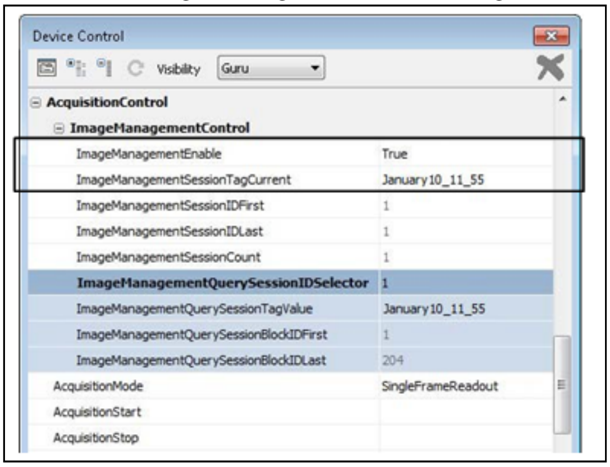
By default, the GenICam features for image management will appear as {Not available}. It is required to set the GenICam feature GevGVSPExtendedIDMode=Off (under TransportLayerControl/GigEVision) to allow enabling image management.

When image management is enabled, image acquisition operates in a slightly different manner than described previously in this guide, with regard to when images are deleted:

- Reading out images from memory does not cause the images to be Images can be read out of memory as many times as required.
- Changing from one acquisition mode to another does not cause the images to be deleted.
- Images remain in memory until the memory is explicitly cleared (by executing BlockBufferClear) or the embedded video interface is restarted or power When the memory is full, the oldest images are overwritten with new images.

To enable image management and specify a session name

1. Start eBUS Player and click **Select/Connect**.
2. Click the device in the **Available Devices**
3. Click **OK** in the bottom right corner.
4. Under **Parameters and Controls** click **Device control**.
5. Under **AcquisitionControl** > **Image Management Control**, set the **ImageManagementEnable** feature to **True**.
6. Beside the **ImageManagementSessionTagCurrent** feature, enter a session name.



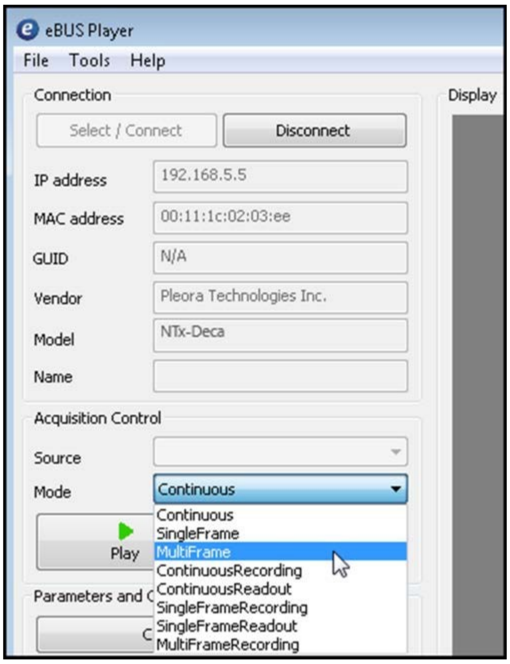
7. Close the **Device Control** dialog box.

Images that were captured before ImageManagementEnable was set to True are not available for retransmission.

To capture images for the acquisition session

1. Ensure you have enabled image management and specified a session name to identify your session, as explained in the previous precedure.
2. On the main screen of eBUS Player, select one of the following acquisition modes in the **Mode** list: **Continuous**, **SingleFrame**, or **MultiFrame**.

> ✅ The acquisition modes are described in "Specifying How Images are Acquired"

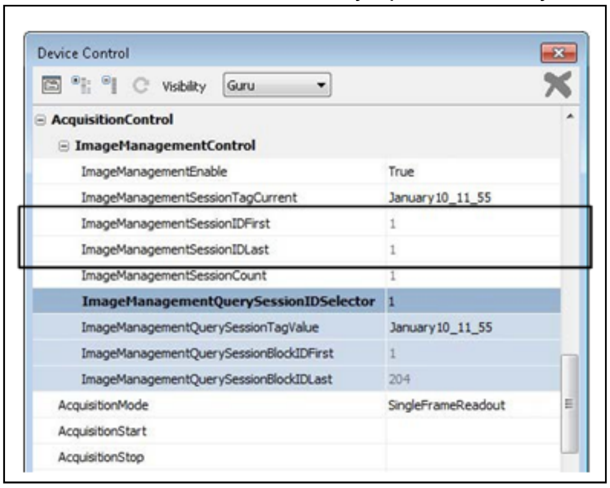


3. Click **Play** to acquire
4. When the session is complete, click **Stop**.

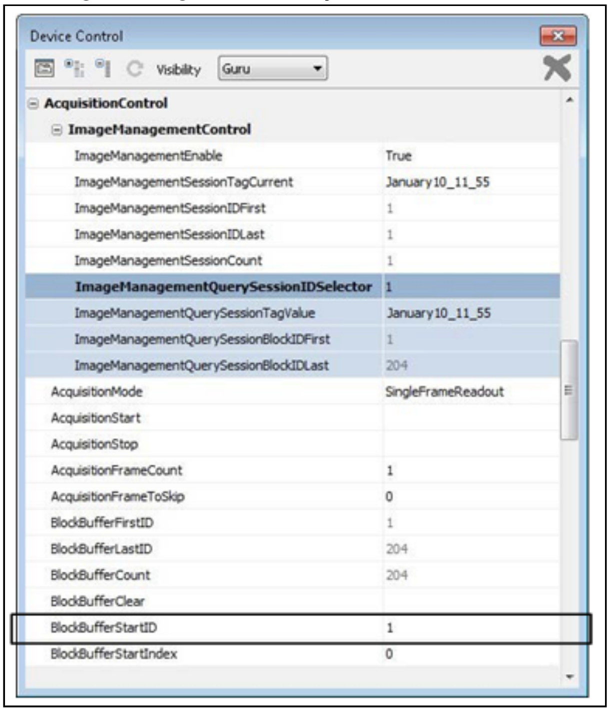
To retrieve images from an acquisition session

1. Under **Parameters and Controls** click **Device control**.
2. Under **Acquisition Control** > **Image Management Control**, verify that **ImageManagementQuerySessionTagValue** shows the session that you are interested in.
   If you want to choose a different session, change the **ImageManagementQuerySessionIDSelector** value.
3. Take note of the values in the following fields, depending on whether you want to retrieve the first or last image from the session:
   - **ImageManagementQuerySessionBlockIDFirst**. Reports the Block ID of the first block for the selected session.
   - **ImageManagementQuerySessionBlockIDLast**. Reports the Block ID of the last block for the selected session.

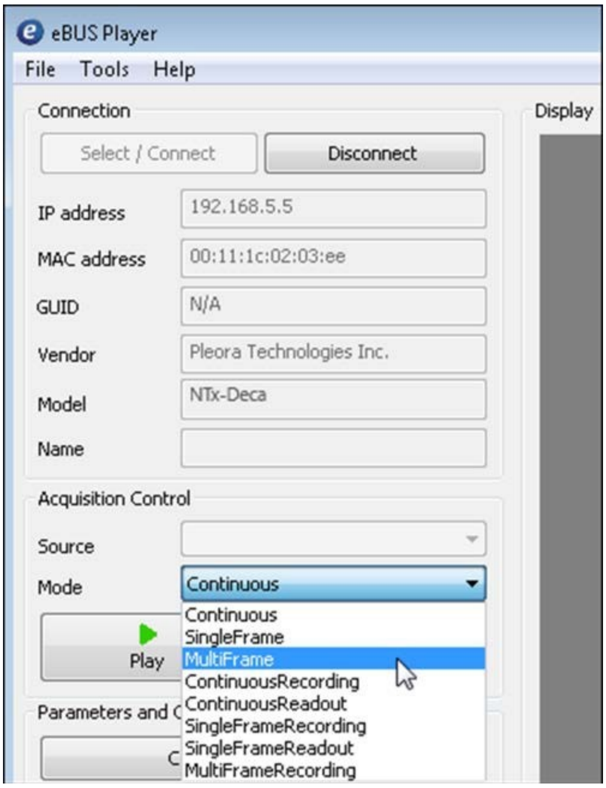
Note that these values are only updated after you stop acquisition.



4. Set **BlockBufferStartID** to the value from **ImageManagementQuerySessionBlockIDFirst** or **ImageManagementQuerySessionBlockIDLast**, or a particular block ID within this range.



5. On the main screen of eBUS Player, select **ContinuousReadout, SingleFrameReadout, or MultiFrameReadout** in the **Mode** list.



6. Click **Play** to retrieve (readout) the images. When the session is complete, click **Stop**.

> You can retrieve the images as many times as you If you are using **Single Frame Readout** mode, re-enter the block ID beside the **BlockBufferStartID** feature and click **Play**.

To clear the embedded or video interface memory

- Under **ImageAcquisition**, click **BlockBufferClear**.

> Resetting or power cycling the embedded video interface will also remove any recorded images from memory.

Table 32: Image Management Features

Name	Description, notes
BlockBufferStartID	Sets the starting Block ID in the Video Interface memory for acquisition readout. The range of Block ID is bounded by the BlockBufferFirstID and BlockBufferLastID.

BlockBufferStartIndex	Sets the starting index of block(s) in the Video Interface memory for acquisition readout. An index of 0 refers to the oldest block in the Video Interface memory.
BlockBufferFirstID	Reports the block ID of the first block in the Video Interface memory. Returns 0 when the memory is empty.
BlockBufferLastID	Reports the block ID of the last complete block in the Video Interface memory. Returns 0 when the memory is empty.
BlockBufferClear	Resets the acquisition path which includes the logic handling of the acquisition, the streaming and all Block ID pointers. Available when ImageManagementEnable = True.
ImageManagementEnable	Enables the Image Management feature. Setting the value to False will reset all Image Management features to the default settings.
ImageManagementSessionTagCurrent	User-defined Session Tag for the current acquisition session.
ImageManagementSessionIDFirst	Reports the Session ID of the first acquisition session in the Video Interface memory.
ImageManagementSessionIDLast	Reports the Session ID of the last acquisition session in the Video Interface memory.
ImageManagementSessionCount	Reports the number of acquisition sessions available in the Video Interface memory.
ImageManagementQuerySessionIDSelector	Selects the Session ID to query information about an acquisition session. The Session ID range is specified by the ImageManagementSessionIDFirst and ImageManagementSessionIDLast.
ImageManagementQuerySessionTagValue	Reports the Session Tag associated with the selected Session ID in the ImageManagementQuerySessionIDSelector.
ImageManagementQuerySessionBlockIDFirst	Reports the Block ID of the first block in the selected Session ID in the ImageManagementQuerySessionIDSelector.
ImageManagementQuerySessionBlockIDLast	Reports the Block ID of the last block in the selected Session ID in the ImageManagementQuerySessionIDSelector.

10.8 Using the Automatic Internal Retrigger Feature to Generate Image Strips

The **AutomaticInternalRetrigger** feature allows you to send strips of data to the host for pre-processing based on a larger image size. The **EOFByLineCount** feature is used to identify the last strip.

The following tables provide examples of subdividing an image into strips. In the first example, assume that images are rendered on the pixel bus with dimensions of 640x480, but strips of 640x100 are required. With this configuration, the device generates five blocks for each image on the pixel bus. The first four blocks have the **EOFByLineCount** flag set so that they end after 100 lines. The fifth block will not have the flag set, so that it ends at the end of the image. Note that in this case the fifth strip is smaller than the others.

Table 33:

Image on pixel bus	Image strip coordinates	Block ID	Block Dimension	EOFByLineCount	LineMIssing
Image 640x480	1,1 - 640,100	1	640x100	1	0
	1,101 - 640,200	2	640x100	1	0
	1,201 - 640,300	3	640x100	1	0
	1,301 - 640,400	4	640x100	1	0
	1,401 - 640,480	5	640x80	0	1

In the next example, assume that images are rendered on the pixel bus with dimensions of 640x500, and again strips of 640x100 are required. The NTx-Deca is again configured to generate strips of 640x100. In this case, the device generates 6 blocks for each image on the pixel bus. The first five blocks will have the **EOFByLineCount** flag set so that they end after 100 lines. The sixth block will not have the flag set. In this case the last strip does not contain any lines.

Table 33

Image on pixel bus	Image strip coordinates	Block ID	Block Dimension	EOFByLineCount	LineMIssing
Image 640x500	1,1 - 640,100	1	640x100	1	0
	1,101 - 640,200	2	640x100	1	0
	1,201 - 640,300	3	640x100	1	0

	1,301 - 640,400	4	640x100	1	0
	1,401 - 640,500	5	640x100	1*	0
		6	0x0	0*	1

*Note that the empty block is only seen if FVAL is de-asserted after LVAL on the pixel bus. In a case where FVAL is de-asserted at the same clock cycle as LVAL, **EOFByLineCount** will be 0 for the fifth block and there will be no empty block at the end.

10.8.1 Setting Up the Automatic Internal Retrigger Feature Using eBUS Player

The following steps show how to set up the automatic internal retrigger feature for the NTx-Deca and verify the **EOFByLineCount** flag. This procedure assumes that a 640x480 image is on the pixel bus and the required strips are 640x100.

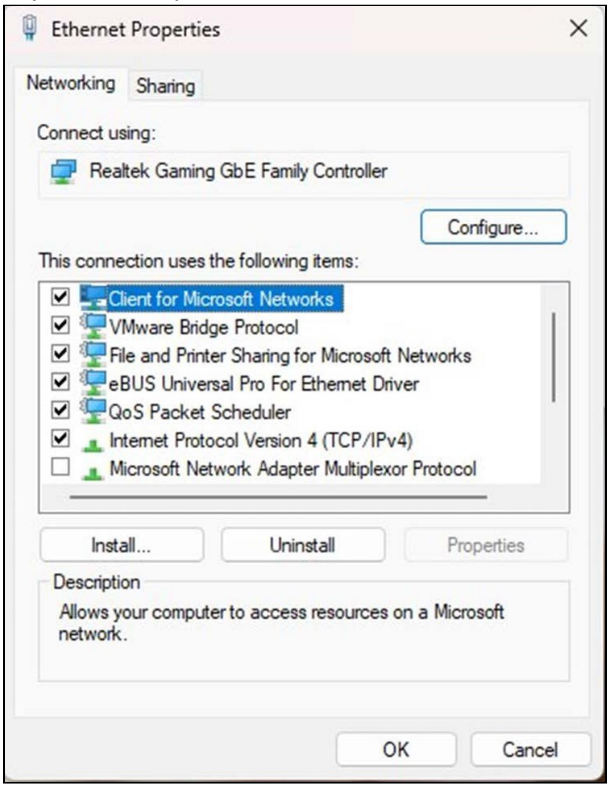
Prerequisites: Install the following tools on the PC that you will be connecting to the NTx-Deca.

- eBUS Player
- Wireshark

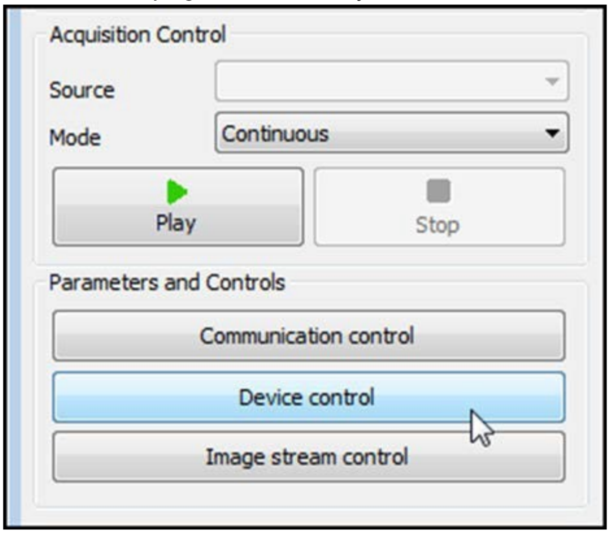
To set up the automatic internal retrigger feature

1. Disable the eBUS Universal Pro for Ethernet Driver on the NIC that you will be connecting to the NTx-Deca.
   Whis is only required to capture GVSP packets with Wireshark.
   It is NOT required to use the Automatic Internal Retrigger functionality directly. This will allow you to

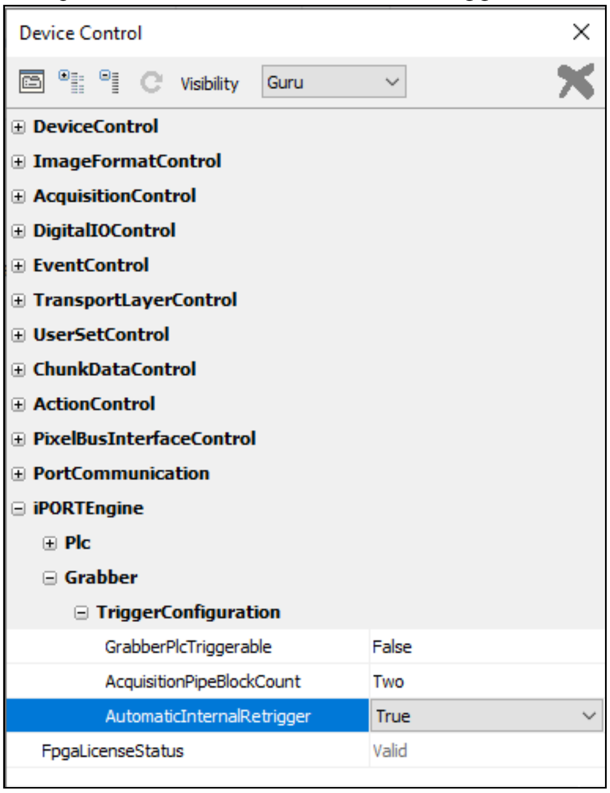
capture GVSP packets with Wireshark.



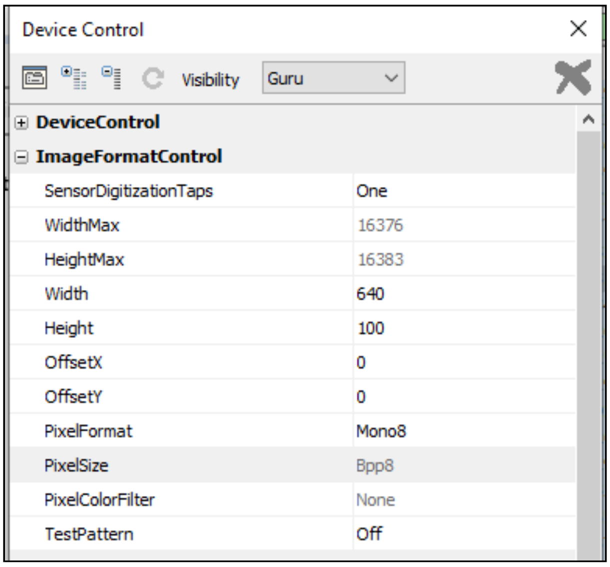
2. Connect to the NTx-Deca using eBUS Player.
3. On the main page of eBUS Player, select **Device control**.



4. Navigate to the **AutomaticInternalRetrigger** feature and set it to **True**.



5. Under **ImageFormatControl**, do the following:
   - Set **Width** to **640**.
   - Set **Height** to **100**.
   - Set **TestPattern** to **Off**.



6. Pleora recommends setting the **AcquisitionPipeBlockCount** setting to **LimitedByOnBoardMemory** if the data rate on the pixel bus is higher than the data throughput that the NTx-Deca can sustain on the Ethernet For example, if the **DeviceLinkSpeed** is downgraded to 5G, 2.5G, or 1G, and the data rate on the pixel bus is above the link speed, the setting is required. Also, even if the **DeviceLinkSpeed** is 10Gbps, and the data rate on the pixel bus is approaching 10Gbps, the setting may be required.

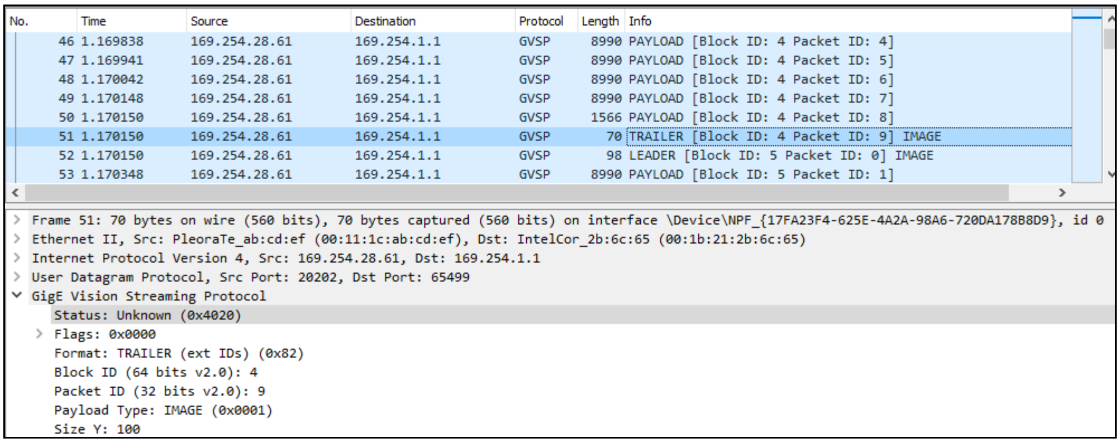
> ✅ Set the **LimitedByOnBoardMemory** setting only if the amount of image data you are acquiring does not exceed the amount of images that can be stored in memory as explained in section "Calculating How Many Images Can be Stored in Onboard Memory"

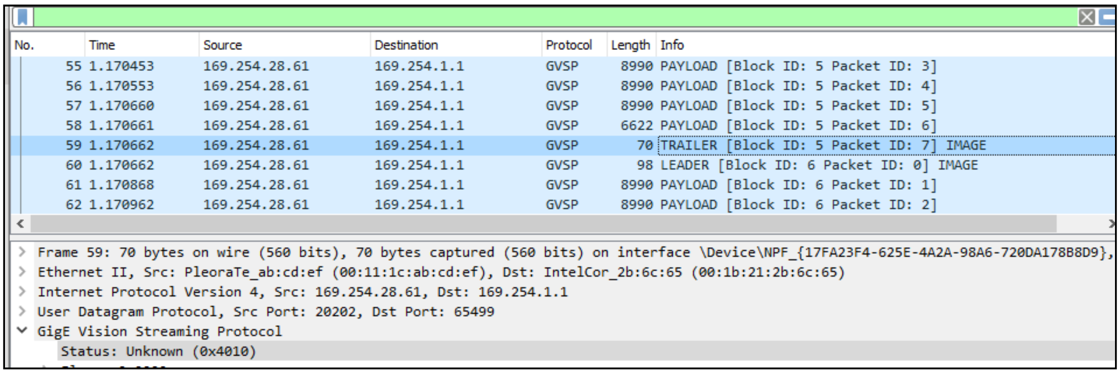
7. Under **AcquisitionControl**, do the following:
   - Set **AcquisitionMode** to **Continuous** or **MultiFrame**.
   - If **AcquisitionMode** is set to **MultiFrame**, set the **AcquisitionFrameCount** to be proportional to the number of expected strips.
8. Start a Wireshark trace on the NIC that is connected to the NTx-Deca and then select **Play**. Capture packets for 2 seconds and then stop the trace.
9. Analyze the You will see that the GigE Vision status code of the data trailer indicates the status of the **EOFByLineCount** flag.
   - **0x4020** is the status code for **EOFByLineCount** flag.
   - **0x4010** is the status code for **LineMissing**

   Table 35:

Block ID	Trailer Status Code	Notes
1	0x4020	Indicates that the **EOFByLineCount** flag is set.
2	0x4020	Indicates that the **EOFByLineCount** flag is set.
3	0x4020	Indicates that the **EOFByLineCount** flag is set.
4	0x4020	Indicates that the **EOFByLineCount** flag is set.
5	0x4010	Indicates that lines are missing, since a 640x100 image was expected but a 640x80 image was received.

Below are some image captures.





10. When you are done, enable the eBUS Universal Pro for Ethernet driver.

10.9 Implementing the eBUS SDK

You can create your own image acquisition software for the NTx-Deca. Consult the following guides for information about creating custom image acquisition software:

- *eBUS SDK API Quick Start Guides*, available for C++, Python, .NET and Linux
- *eBUS SDK API Help Files*

11 Network Configurations for the NTx-Deca

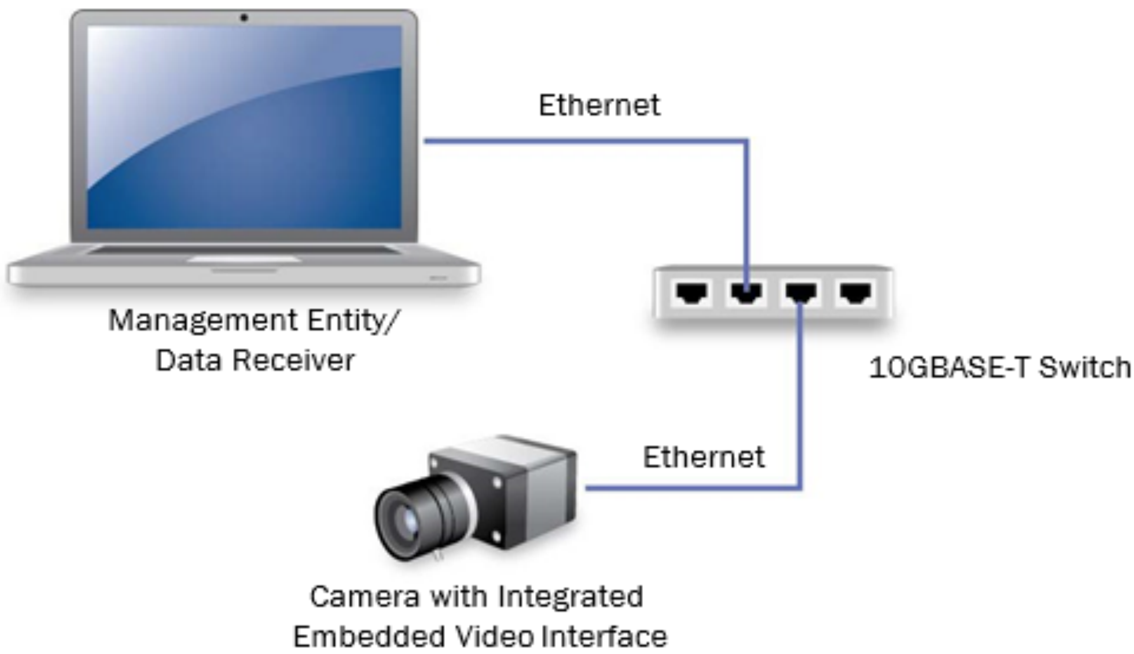
After you have connected to the NTx-Deca and provided it with a unique IP address on your network, you can configure the NTx-Deca for either unicast or multicast.

11.1 Unicast Network Configuration

In a unicast configuration, an NTx-Deca is connected to a 10GBASE-T switch that sends a stream of images over Ethernet to the computer. Alternatively, the NTx-Deca can be connected directly to the computer.

The computer is configured as both a data receiver and controller, and serves as a management entity for the NTx-Deca.

Figure 11: Unicast Network Configuration NTx-Deca



11.1.1 NTx-Deca Required Items — Unicast Network Configuration

You require the following components to set up a unicast network configuration:

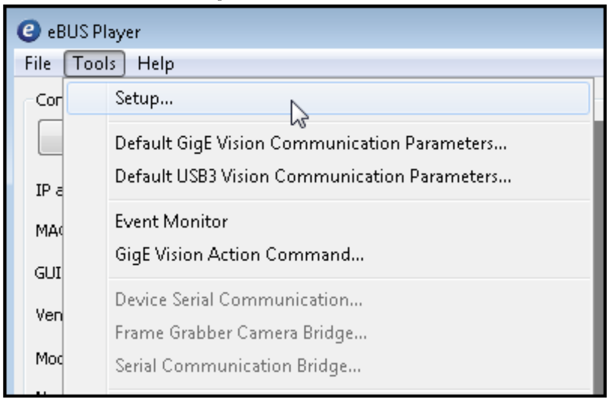
- Imaging device with integrated NTx-Deca and cables
- CAT6a or CAT7 Ethernet cable (quantity: 1)
- 10GBASE-T switch and an additional CAT6a or CAT7 Ethernet cable (optional)
- Desktop computer or laptop with eBUS SDK, version 6.2 (or later) installed, and 10GBASE-T Ethernet ports, which are required for optimal performance

11.1.2 NTx-Deca Configuration — Unicast Network Configuration

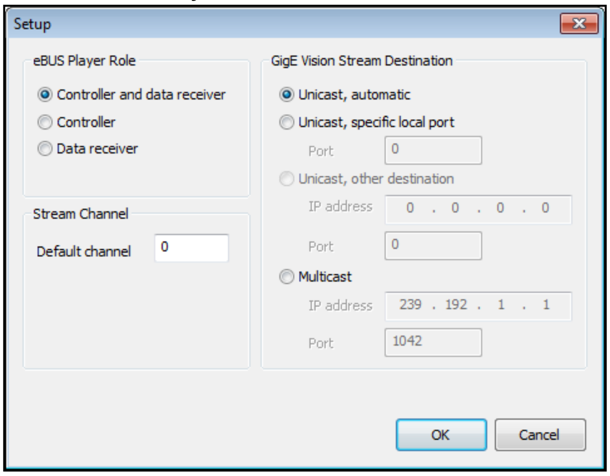
After you have connected and applied power to the hardware components, use eBUS Player to configure the NTx-Deca Embedded Video Interface for a unicast network configuration.

To configure the NTx-Deca for a unicast network configuration

1. Start **eBUS Player**.
2. Click **Tools > Setup**.

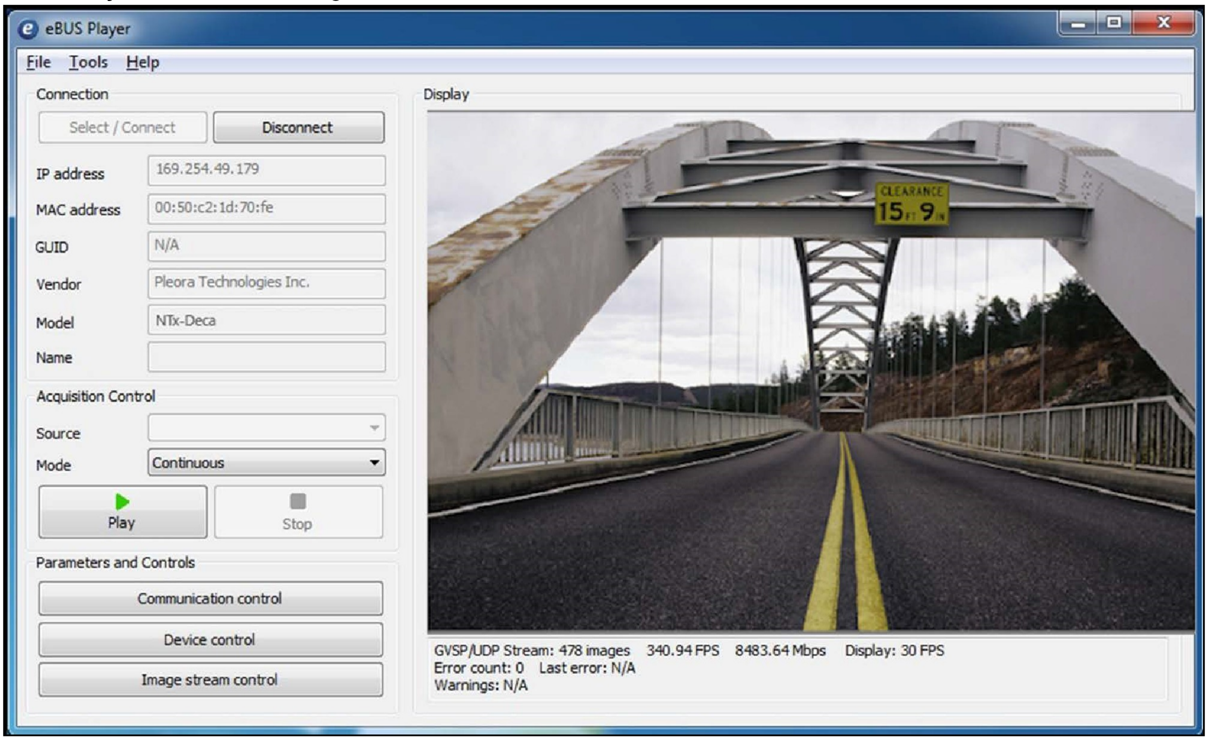


3. Under **eBUS Player Role**, click **Controller and data receiver**.



4. Under **GigE Vision Stream Destination**, click **Unicast, automatic**.
5. Click **OK**.
6. Connect to the NTx-Deca
   For more information, see “To start eBUS Player and connect to a device”

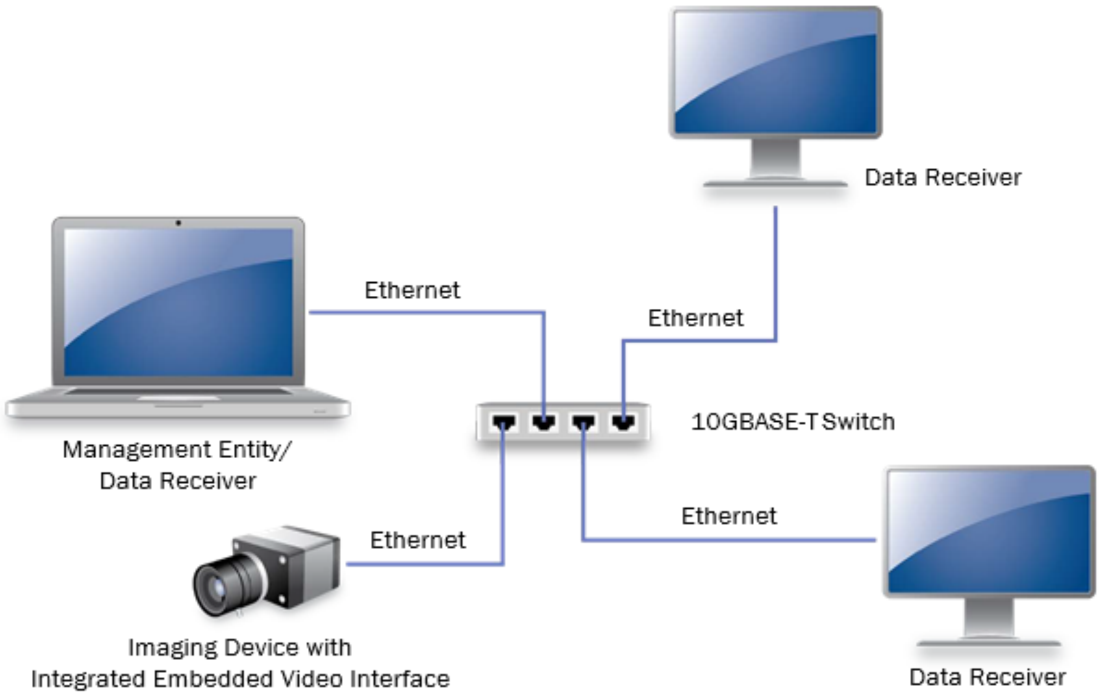
7. Click **Play** to view a live image stream.



11.2 Multicast Network Configuration

In a multicast network configuration, the NTx-Deca is connected to a 10GBASE-T switch, and sends a stream of images over Ethernet simultaneously to multiple receiving computers.

Figure 12: Multicast Network Configuration



11.2.1 Required Items — Multicast Network Configuration

You require the following components to set up a multicast network configuration:

- Imaging device with integrated NTx-Deca and cables
- CAT6a or CAT7 Ethernet cables
- 10GBASE-T switch
- 1 desktop or laptop computer* to manage the embedded video interface and receive the multicast image stream
- 1 or more desktop or laptop computers* to receive the multicast image stream

*Ensure the computers are running eBUS SDK, version 6.2 (or later)

11.2.2 Connecting the Devices

This section lists the physical connections that must be made.

To connect the device

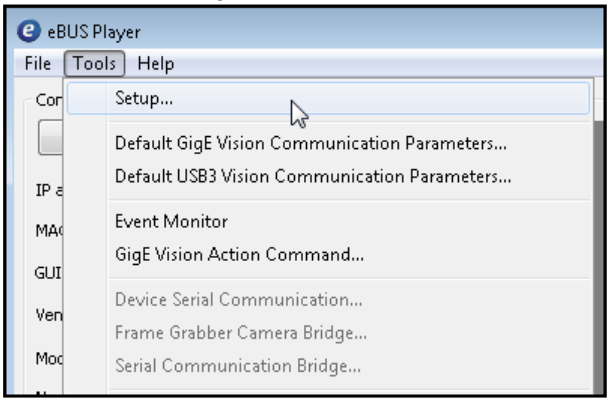
1. Using CAT6a/CAT7 cables, connect the computers to available ports on the 10GBASE-T switch.
2. Using a CAT6a/CAT7 cable, connect the iPORT NTx-Deca to an available port on the 10GBASE- T switch.
3. Apply power to the devices.

11.2.3 Configuring the Devices for a Multicast Network Configuration

This section lists the physical connections that must be made.

To configure a receiving computer to receive the multicast image stream

1. On the computer that you want to receive the multicast image stream, start **eBUS Player**.
2. Click **Tools** > **Setup**.



3. Under **eBUS Player Role**, click **Data receiver**.
4. Under **GigE Vision Stream Destination**, click **Multicast** and enter the **IP address** and **Port**. For example, 192.1.1.
5. Click **OK.**
   At this moment, the **Display** section of eBUS Player will be inactive because the image stream has not yet been multicast out from the embedded video interface.

   Note: Repeat this procedure for other computers that you want to receive the multicast image stream.

To configure the embedded video interface to multicast the image stream to receiving computers

1. On the computer that you are using to manage the embedded video interface, start **eBUS Player**.
2. Click **Tools > Setup**.
3. Under **eBUS Player Role**, click **Controller and data receiver**.
4. Under **GigE Vision Stream Destination**, click **Multicast** and enter the **IP address** and **Port**. The IP address and port must be identical to that configured for the receiving computer(s) in Step 4 of "To configure a receiving computer to receive the multicast image stream".
5. Click **OK**.
6. Connect to the embedded video interface,
   For more information, see "To start eBUS Player and connect to a device"
7. Click **Play** to receive the image stream.
   The image stream will be multicast out from the embedded video interface and will appear automatically in eBUS Player on the receiving computers.

12 System Troubleshooting

This chapter provides you with troubleshooting tips and recommended solutions for issues that can occur during configuration, setup, and operation of the iPORT NTx-Deca. It also shows you how to switch between the backup and main firmware loads.

Not all scenarios and solutions are listed here. You can refer to the Pleora Technologies Support Center at www.pleora.com for additional support and assistance. Details for creating a customer account are available on the Pleora Technologies Support Center.

Refer to the product release notes that are available on the Pleora Technologies Support Center for known issues and other product features.

12.1 Troubleshooting Tips

The scenarios and known issues listed in this chapter are those that you might encounter during the setup and operation of your NTx-Deca. Not all possible scenarios and errors are presented. The symptoms, possible causes, and resolutions depend upon your particular network, setup, and operation.

If you perform the resolution for your issue and the issue is not corrected, we recommend you review the other resolutions listed in this table. Some symptoms may be interrelated.

Table 36: Troubleshooting Tips

Symptom	Possible cause	Resolution
SDK cannot detect or connect to the NTx-Deca	Power not supplied to the iPORT NTx-Deca, or inadequate power supplied	Both the detection and connection to the NTx- Deca will fail if adequate power is not supplied to the device. Re-try the connection to the device with eBUS Player. Verify that the status LED (D1) is on. For information about the status LED, see "Status LEDs" on page 25.

	Device is not connected to the network	Verify that the network activity LED and network connection speed LED (J6) are active. If these LEDs are illuminated, check the LEDs on your network switch to ensure the switch is functioning properly. If the problem continues, connect the NTx-Deca directly to the computer to verify its operation. For information about the network LEDs, "Status LEDs" on page 25.
	The iPORT NTx-Deca and computer are not on the same subnet	Images might not appear in eBUS Player if the NTx-Deca and the computer running eBUS Player are not on the same subnet. Ensure that these devices are on the same subnet. In addition, ensure that these devices are connected using valid gateway and subnet mask information. You can view the NTx-Deca IP address information in the Available Devices list in eBUS Player. A red icon appears beside the device if there is an invalid IP configuration.
SDK is able to connect, but no images appear in eBUS Player.	In a multicast configuration, the NTx-Deca may not be configured correctly	Images might not appear on the display if you have not configured the NTx-Deca for a multicast network configuration. The NTx-Deca and all multicast receivers must have identical values for both the GevSCDA and GevSCPHostPort features in the TransportLayerControl section. For more information, see "Multicast Network Configuration" on page 109.
	In a multicast configuration, your computer's firewall may be blocking eBUS Player	Ensure that eBUS Player is allowed to communicate through the firewall.
	Anti-virus software or firewalls blocking transmission	Images might not appear in eBUS Player because of anti-virus software or firewalls on your network. Disable all virus scanning software and firewalls, and re-attempt a connection to the NTx-Deca with eBUS Player.

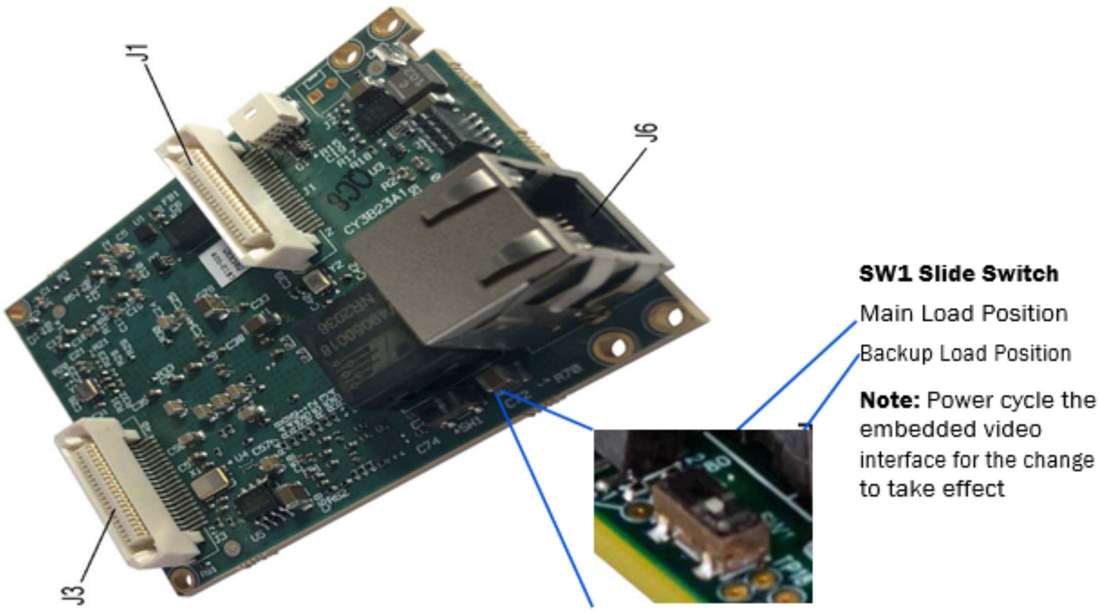
12.2 Changing to the Backup Firmware Load

In the event that the main firmware load fails to load, the NTx-Deca will start up using the backup firmware load when it is restarted or power cycled.

In the rare event that the backup load is not used automatically (as indicated by the fact that eBUS Player will not be able to detect the NTx-Deca), you can use the slide switch to change to the backup load.

After the NTx-Deca starts up using the backup load, you can apply a firmware update to the NTx-Deca to recover the main load. For more information see the *Updating Pleora Firmware* knowledge base article on the Pleora Support Center (https://supportcenter.pleora.com/).

Slide switch (SW1) location


J1
J6
J3
SW1 Slide Switch
Main Load Position
Backup Load Position
Note: Power cycle the embedded video interface for the change to take effect

13 Reference: Mechanical Drawings and Material List

This chapter provides mechanical drawings and also provides a list of connectors and cables, with corresponding manufacturer details.

Three-dimensional (3-D) mechanical drawings are available at the Pleora Technologies Support Center.

13.1 NTx-Deca Mechanical Drawings

The mechanical drawings in this section provide the NTx-Deca ’s dimensions, features, and attributes. All dimensions are in millimeters.

Figure 13: NTx-Deca Component Height — Top View

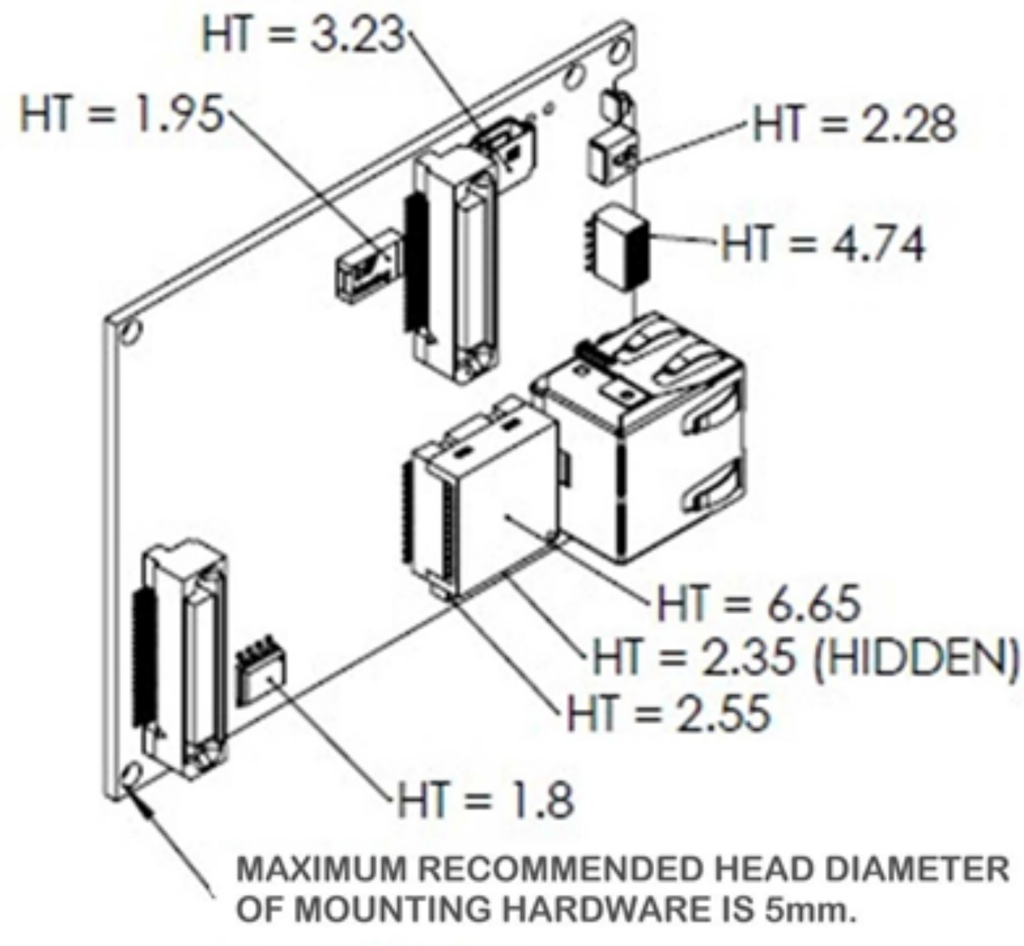


Figure 14: NTx-Deca Component Height — Bottom View

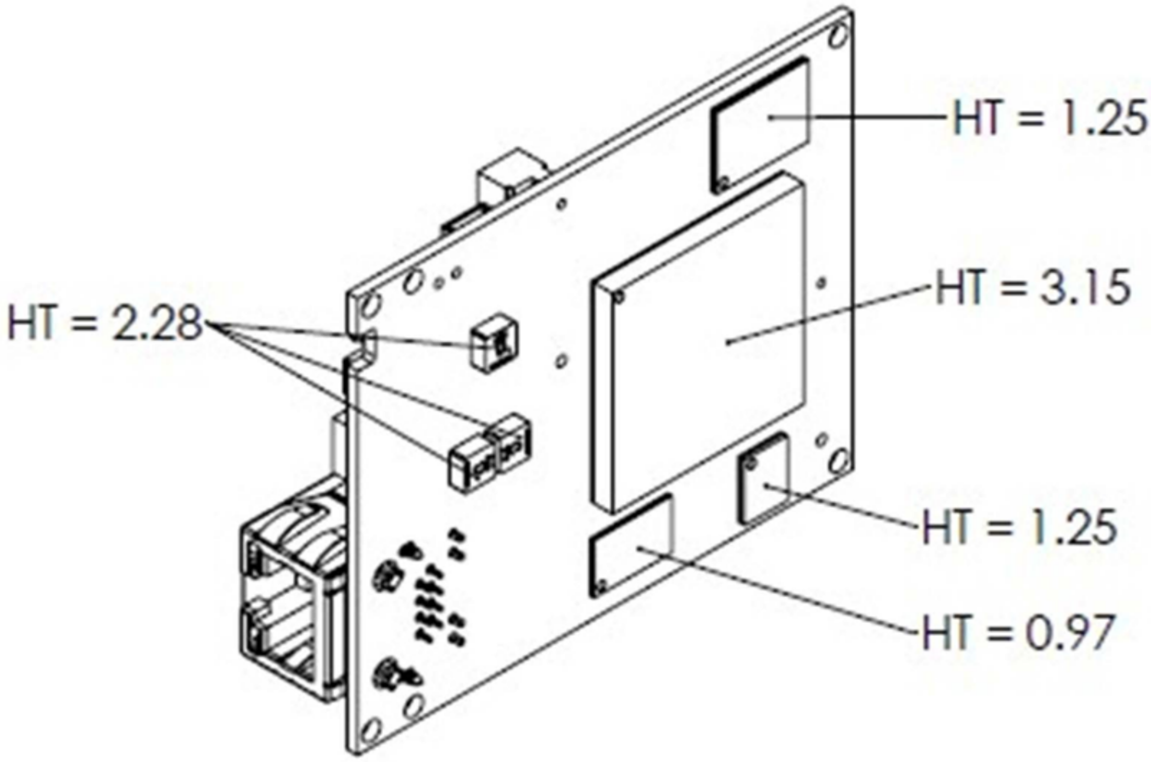


Figure 15: NTx-Deca — Bottom View

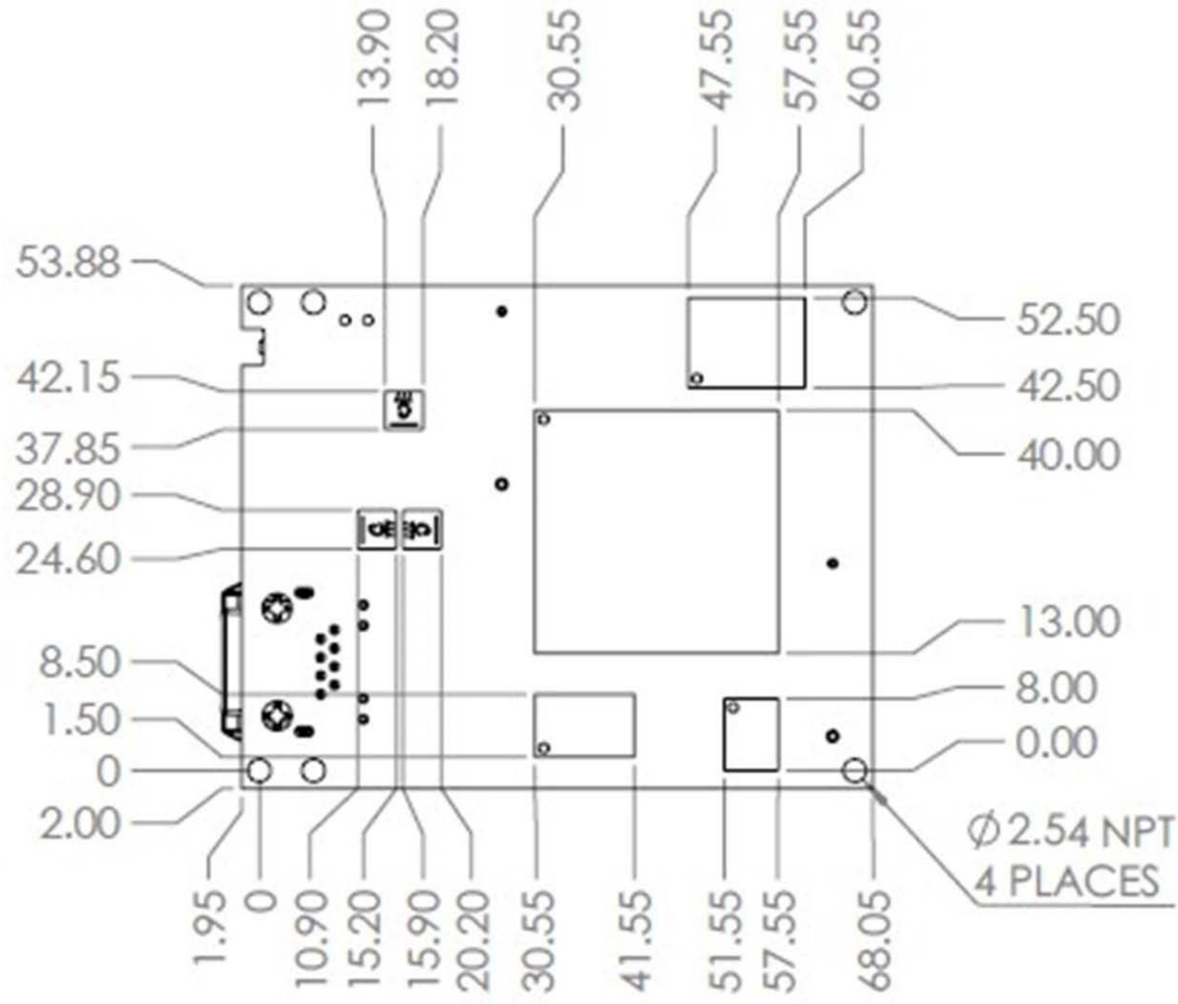


Figure 16: NTx-Deca — Top View

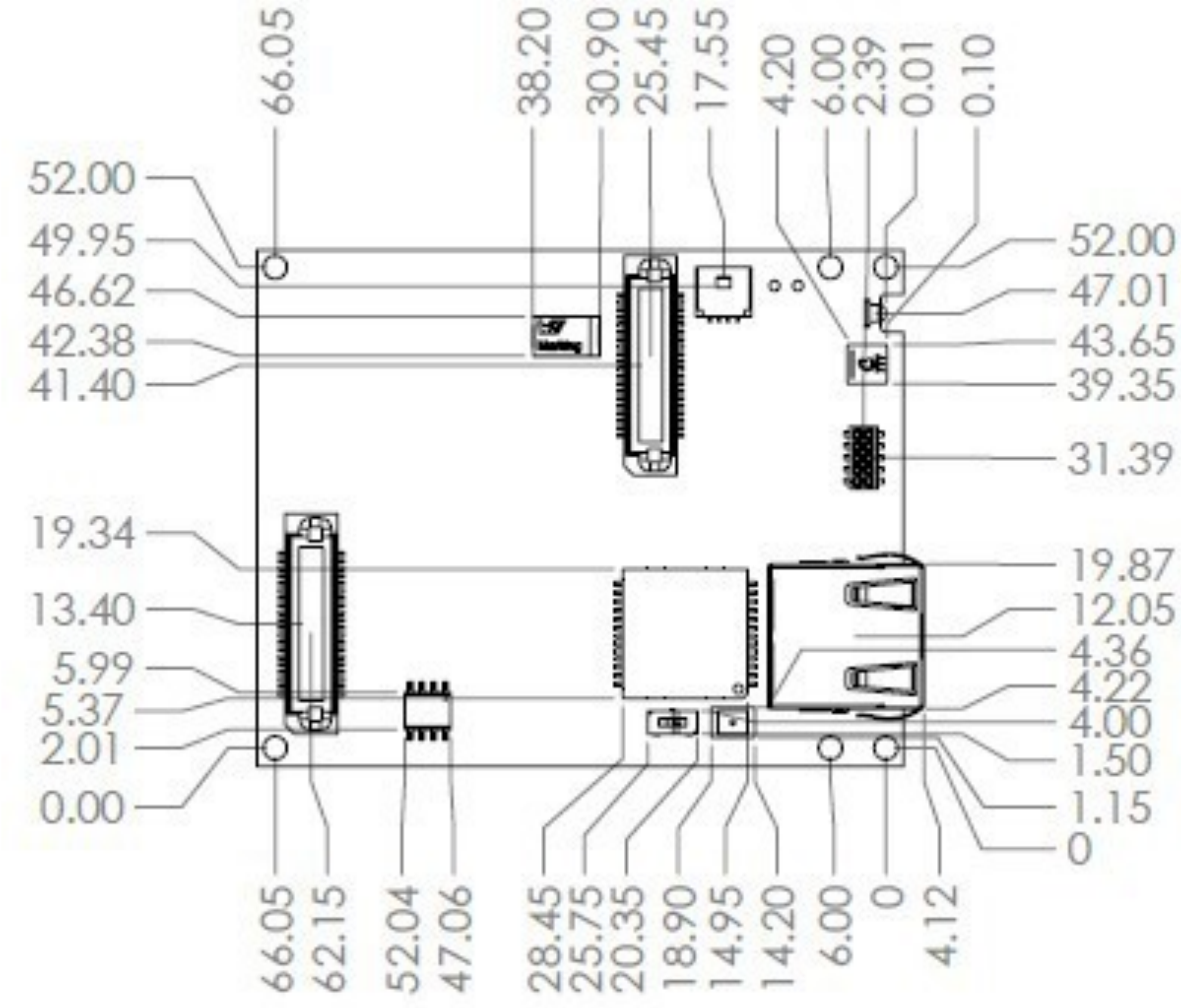


Figure 17: NTx-Deca — Side Views

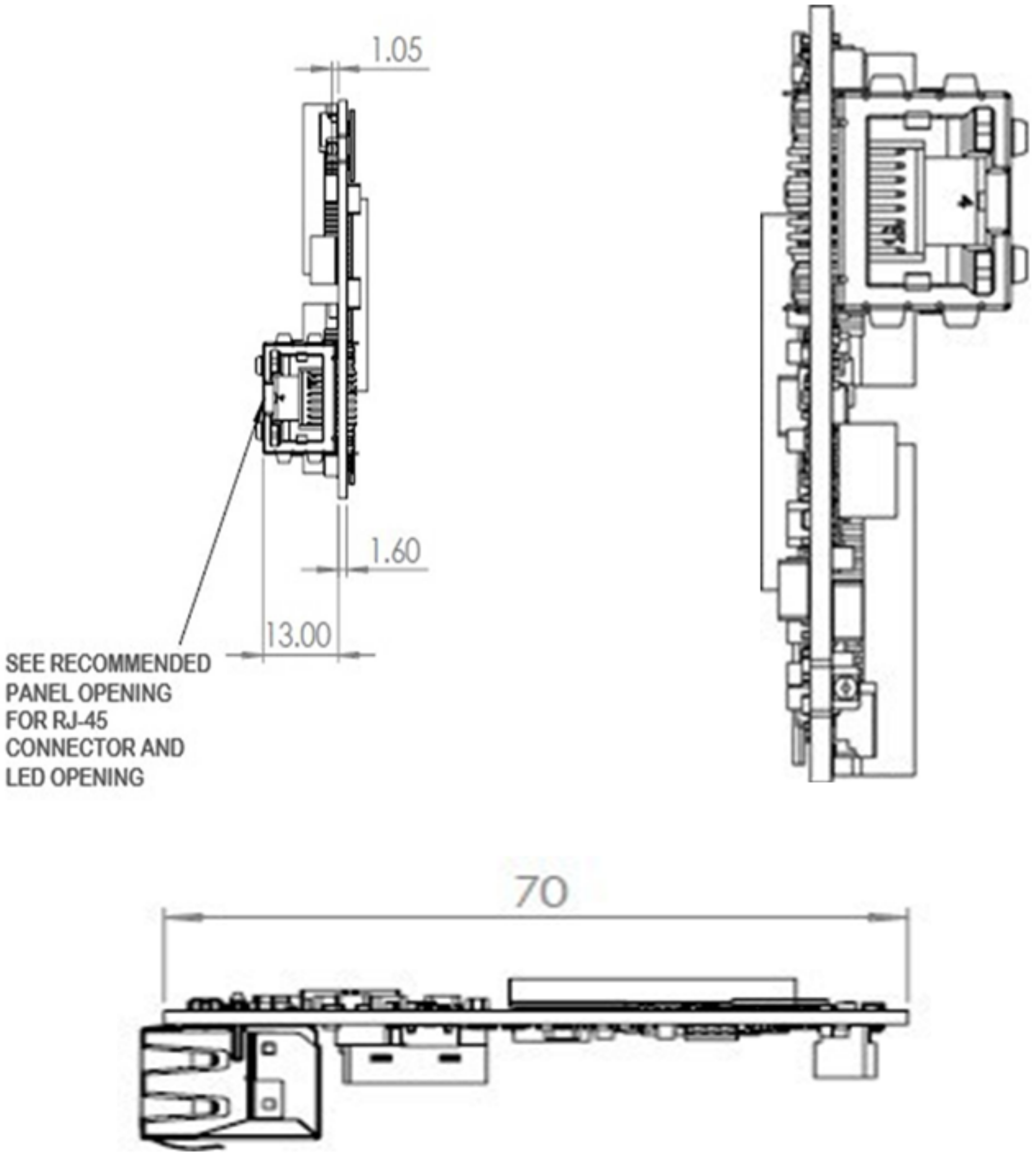
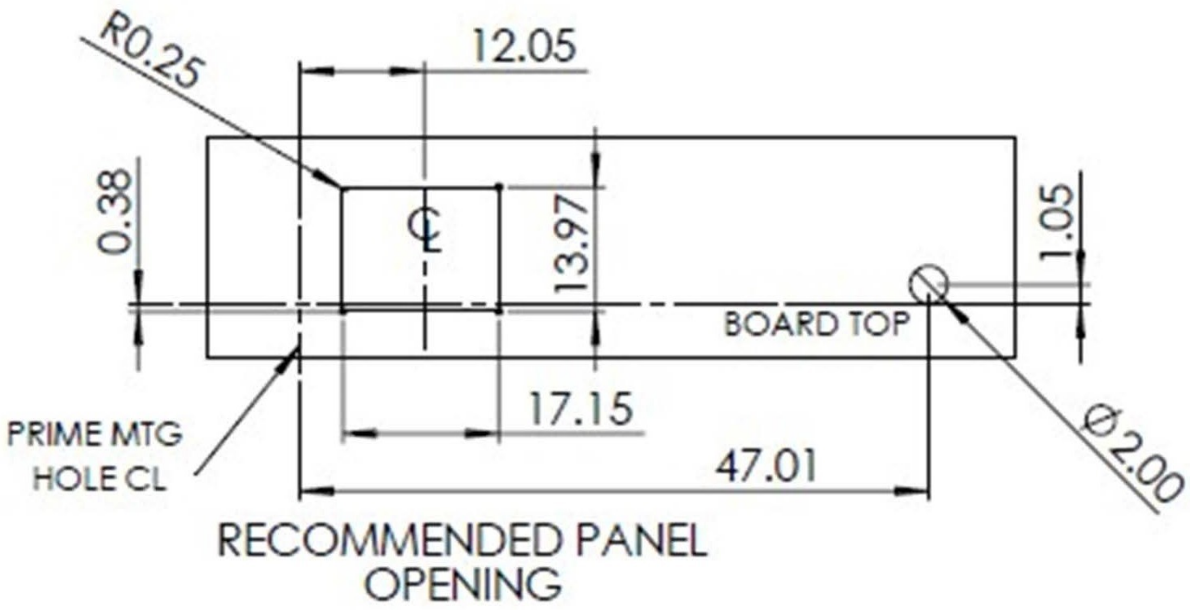


Figure 18: Recommended Ethernet Jack Panel Opening



13.2 Material List

The connector summaries for the NTx-Deca are listed in the following table.

ID	Description	Manufacturer part number	Manufacturer
J1, J3	40-pin user circuitry connector	FX6-40S-0.8SV2(93)	Hirose
J6	RJ-45 Ethernet connector	SS-60300-101	Stewart Connector

Source manufacturer, description, and identification may vary and are subject to change for each connector.

13.2.1 Screw and Mechanical Information

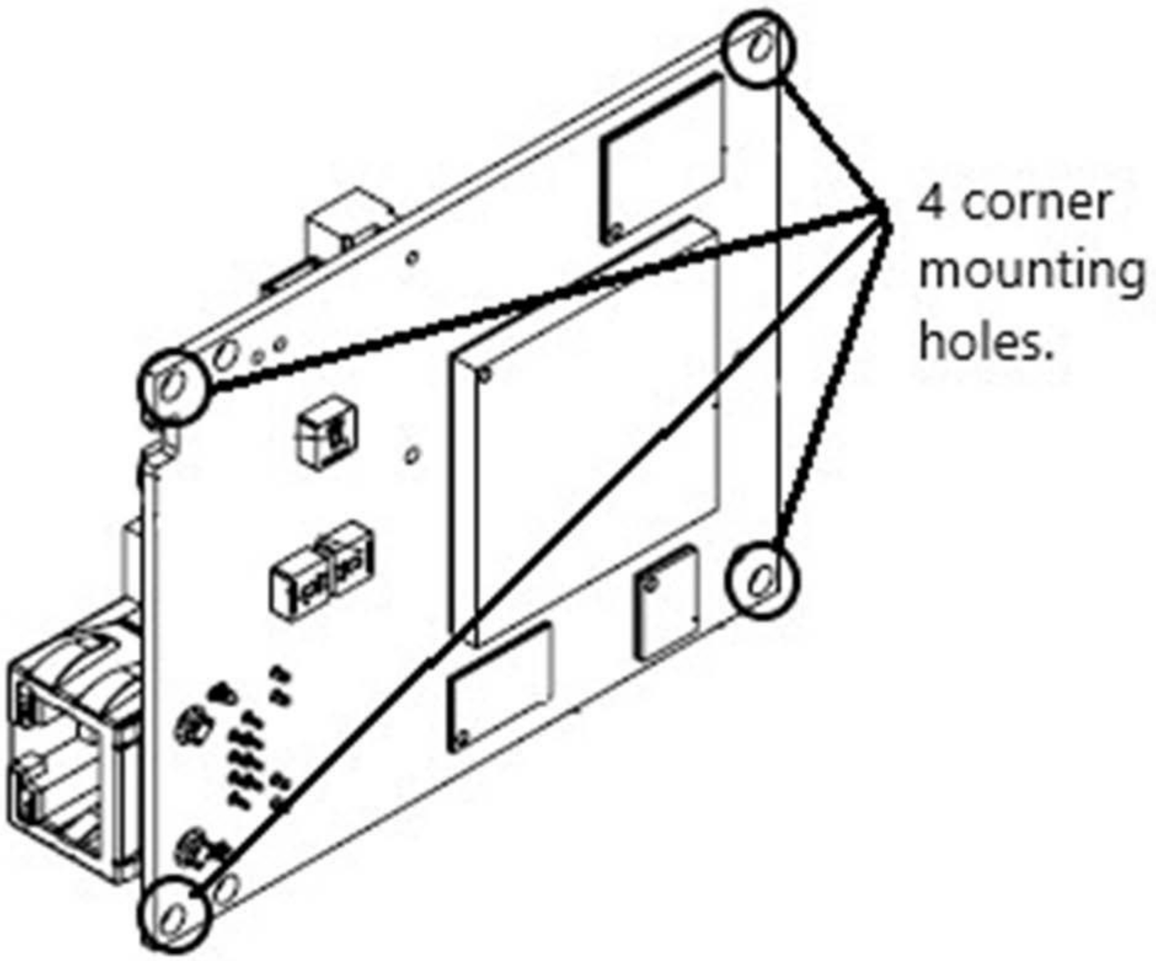
Metric:

Size	Type	Maximum Torque

M2.5	Screw: Pan head, 5 mm maximum head diameter.	0.5 Nm
	Hex nut: 5 mm maximum flat to flat on secondary board side only.	
	Hex standoff: 4.5 mm maximum flat to flat.	
	Stainless steel washer: 5 mm maximum outer diameter, 2.7 mm inner diameter.	
	Nylon plastic washer: 5 mm maximum outer diameter, 2.7 mm inner diameter.	

Imperial:

Size	Type	Maximum Torque
2-56	Screw: Pan head, 0.167 inch maximum head diameter.	3.5 in-lbs
	Hex nut: 3/16 inch maximum flat-to-flat on secondary board side only..	
	Hex standoff: 3/16 inch maximum flat-to-flat on secondary board side only or 1/8 inch maximum flat-to-flat on primary or secondary side.	
	Stainless steel washer: 0.188 inch maximum outer diameter, 0.094 inch inner diameter.	
	Nylon plastic washer: 0.188 inch maximum outer diameter, 0.094 inch inner diameter.	



⚠ Only the 4 corner mounting holes should be used for mounting of the NTx-Deca.

Technical Support

On the Pleora Support Center, you can:

- Download the latest software and firmware.
- Log a support issue.
- View documentation for current and past releases.
- Browse for solutions to problems other customers have encountered.
- Read knowledge base articles for information about common tasks.

To visit the Pleora Support Center:

- Go to supportcenter.pleora.com.

- Most material is available without logging in to a Support Center account.
- To access software and firmware downloads, in addition to other content, log in to the Support Center.
- If you do not have an account, click Request Account.
- Accounts are usually validated within one business day.

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