PLEORA TECHNOLOGIES INC.

iPORT™ NTx-U3 Embedded Video Interface
User Guide

Pleora Technologies

Document Number

EX001-023-0013, Version 1.0 10/5/2019

Table of Contents

Chapter 1

About this Guide

This chapter describes the purpose and scope of this guide, and provides a list of complementary guides.

The following topics are covered in this chapter:

What this Guide Provides

This guide provides you with all of the information you need to connect the iPORT™ NTx-U3 to your sensor and related electronics to create a camera or other imaging device. In this guide you will find a product overview, connector details, and mechanical drawings, along with instructions for installing the Pleora eBUS™ SDK, connecting the device, and performing general configuration tasks to properly display video.

The last chapter of this guide provides Technical Support contact information for Pleora Technologies.

Documented Product Versions

This guide covers the following product versions. The features and functionality documented in this guide may vary if you are using an earlier or later version of the product.

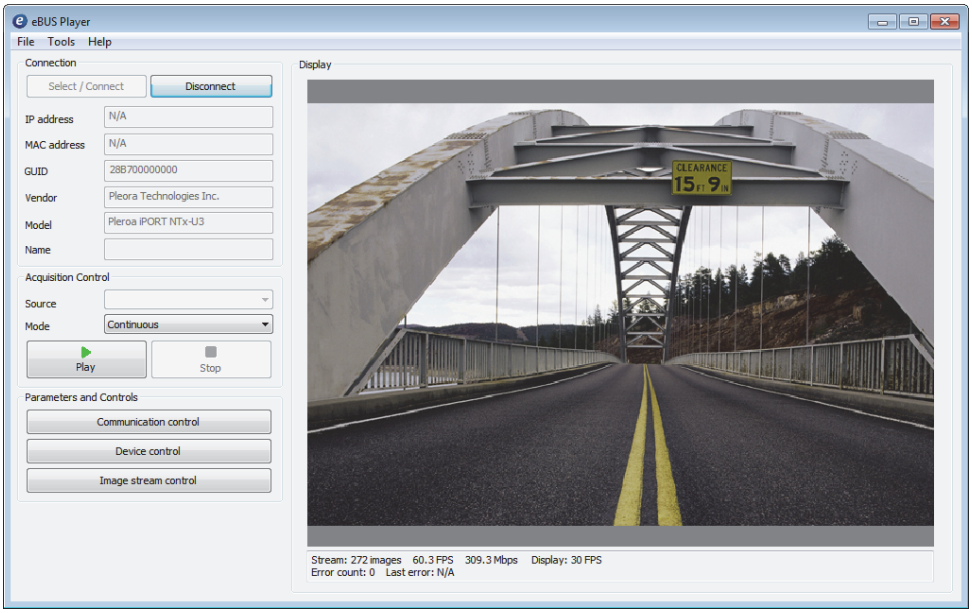
Table 1: Documented Product Versions

Product	Version documented in this guide...
iPORT NTx-U3 External Frame Grabber	1.2.0
eBUS SDK and eBUS Player	6.1

Start Streaming Video

If you want to quickly start streaming video, you can jump to:

- "Confirming Image Streaming" on page 68
- "Configuring the Image Settings" on page 69



Related Documents

The *iPORT NTx-U3 Embedded Video Interface User Guide* is complemented by the following Pleora Technologies documents, which are available on the Pleora Technologies Support Center (supportcenter.pleora.com):

- *eBUS Player Quick Start Guide* and *eBUS Player User Guide,* available for Windows, Linux, and macOS
- *eBUS SDK API Quick Start Guides*, available for C++, .NET, Linux, and macOS
- *iPORT Advanced Features User Guide*
- *Introduction: Establishing a Serial Bridge* knowledge base article

You can also consult the *eBUS SDK API Help Files*, which are installed on your computer during the installation of the eBUS SDK. You can access this documentation from the Windows Start menu under **eBUS SDK**.

Further Reading

Although not required in order to successfully use the NTx-U3, you can find details about industry-related standards and naming conventions in the following documents:

- *USB3 Vision Standard*, available from the AIA at www.visiononline.org
- *GenICam Standard Features Naming Convention*, available from the European Machine Vision Association (EMVA) at www.emva.org.
- *Pixel Format Naming Convention*, available from the EMVA at www.emva.org.

Chapter 2

About the iPORT NTx-U3 Embedded Video Interface

This chapter describes the NTx-U3, including the models and key features.

The following topics are covered in this chapter:

About the NTx-U3 Embedded Video Interface

Pleora's iPORT™ NTx-U3 Embedded Video Interface hardware provides system and camera manufacturers with a straightforward way to integrate USB3 Vision video connectivity into their products.

With the NTx-U3 Embedded Video Interface, manufacturers can shorten time-to-market, reduce development and deployment risk, and lower design and system costs. Pleora's NTx-U3 Embedded Video Interface interacts seamlessly with Pleora's other products in networked or point-to-point digital video systems. It also complies fully with the USB3 Vision™ and GenICam® standards, ensuring interoperability with third-party equipment in a multi-vendor environment. The embedded hardware converts video data to packets at throughputs up to 3 Gb/s. The packetized video is then sent with low, consistent latency over a USB 3.0 link to receiving software.

To speed time-to-market, Pleora offers a Development Kit for the NTx-U3 Embedded Video Interface. This kit allows manufacturers to produce system or camera prototypes and proof-of-concept demonstrations easily and rapidly, often without undertaking hardware development.

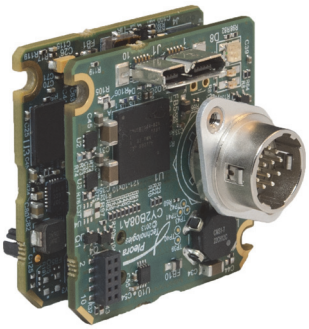
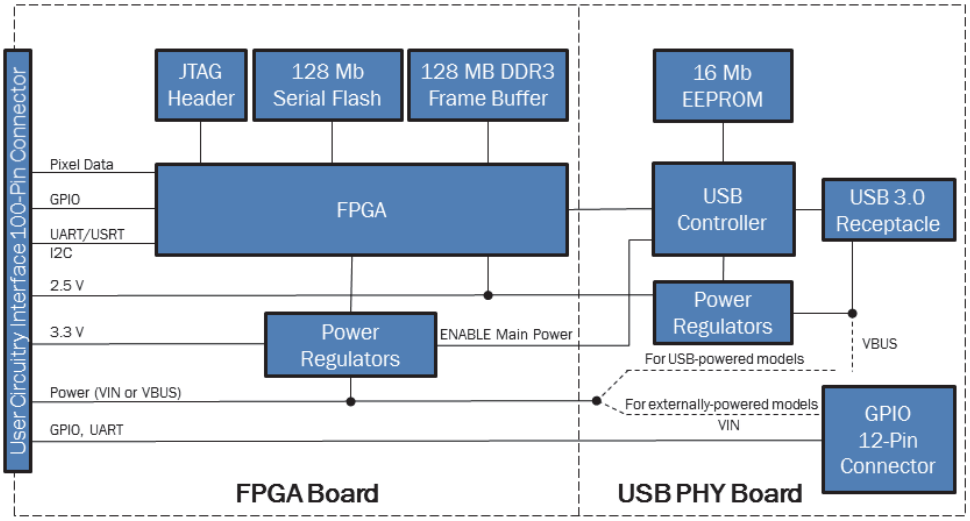


Figure 1: NTx-U3 Block Diagram



Models

The iPORT NTx-U3 is available in several models and is equipped with the parts listed in the following table. Before assembly, ensure that all components are included in the selected package.

Table 2: Models

Order code	Model	Quantity
903-0001	**iPORT NTx-U3 OEM Basic Board Set, USB-powered** *Device Model Name: iPORT-NTx-U3-PT03-PB0UP01-128xU*	
	NTx-U3 OEM basic board set, without 12-pin circular connector	1

Order code	Model	Quantity
903-0002	**iPORT NTx-U3 OEM Board Set, USB-powered** *Device Model Name: iPORT-NTx-U3-PT03-PB0UP01-128xU*	
	NTx-U3 OEM board set, including 12-pin circular connector, soldered on with metal flange	1

Order code	Model	Quantity
903-0003	**iPORT NTx-U3 Development Kit, USB-powered**	
	iPORT NTx-U3 OEM Board Set, USB-powered (903-0002)	1
	NTx-Mini adapter board	1
	Flat flex cables	3
	Prober board	1
	USB 3.0 cable	1
	Pleora eBUS SDK, provided on USB stick (includes eBUS Player sample application)	1

Table 2: NTx-U3 Models (Cont'd)

Order code	Model	Quantity
903-0022	**iPORT NTx-U3-IND OEM Basic Board Set, USB-powered** *Device Model Name: iPORT-NTx-U3-PT03-PB0UP01-128xU*	
	NTx-U3-IND OEM basic board set, without 12-pin circular connector	1

Order code	Model	Quantity
903-0023	**iPORT NTx-U3-IND OEM Board Set, USB-powered** *Device Model Name: iPORT-NTx-U3-PT03-PB0UP01-128xU*	
	NTx-U3- IND OEM board set, including 12-pin circular connector, soldered on with metal flange	1

Order code	Model	Quantity
903-0024	**iPORT NTx-U3-IND Development Kit, USB-powered**	
	iPORT NTx-U3-IND OEM Board Set, USB-powered (903-0023)	1
	NTx-Mini adapter board	1
	Flat flex cables	3
	Prober board	1
	USB 3.0 cable	1
	Pleora eBUS SDK, provided on USB stick (includes eBUS Player sample application)	1

Order code	Model	Quantity
903-0004	**iPORT NTx-U3 OEM Basic Board Set, external-powered** *Device Model Name: iPORT-NTx-U3-PT03-PB0UP01-128xU*	
	NTx-U3 OEM basic board set, without 12-pin circular connector	1

Order code	Model	Quantity
903-0005	**iPORT NTx-U3 OEM Board Set, external-powered** *Device Model Name: iPORT-NTx-U3-PT03-PB0UP01-128xU*	
	NTx-U3 OEM board set, including 12-pin circular connector, soldered on with metal flange	1

Table 2: NTx-U3 Models (Cont'd)

Order code	Model	Quantity
903-0006	**iPORT NTx-U3 Development Kit, external-powered**	
	iPORT NTx-U3 OEM Board Set, external-powered (903-0005)	1
	NTx-Mini adapter board	1
	Flat flex cables	3
	Prober board	1
	Power supply	1
	USB 3.0 cable	1
	Pleora eBUS SDK, provided on USB stick (includes eBUS Player sample application)	1

Order code	Model	Quantity
903-0025	**iPORT NTx-U3-IND OEM Basic Board Set, external-powered** *Device Model Name: iPORT-NTx-U3-PT03-PB0UP01-128xU*	
	NTx-U3 OEM basic board set, without 12-pin circular connector	1

Order code	Model	Quantity
903-0026	**iPORT NTx-U3-IND OEM Board Set, external-powered** *Device Model Name: iPORT-NTx-U3-PT03-PB0UP01-128xU*	
	NTx-U3 OEM-IND board set, including 12-pin circular connector, soldered on with metal flange	1

Order code	Model	Quantity
903-0027	**iPORT NTx-U3-IND Development Kit, external-powered**	
	iPORT NTx-U3-IND OEM Board Set, external-powered (903-0026)	1
	NTx-Mini adapter board	1
	Flat flex cables	3
	Prober board	1
	Power supply	
	USB 3.0 cable	1
	Pleora eBUS SDK, provided on USB stick (includes eBUS Player sample application)	1

Feature Set

Hardware	
User circuitry interface	100-pin Samtec connector: LSHM-150-04.0-L-DV-A-N-TR
External interface	12-pin Hirose connector: HR10A-10R-12PB(71)
USB 3.0 interface, controller	10-pin USB 3.0 Micro-B receptacle Cypress FX3
FPGA	Altera Cyclone V
Image buffer	120 MB 16-bit wide DDR3 Total image size should be smaller than (120 MB-32 k)
Persistent memory	128 Mb serial flash
Clock generator	Included
JTAG header	Connection to FPGA
Inputs/Outputs on User Circuitry Interface	
Video input*	2.5 V, 3.0 V, or 3.3 V LVTTL/LVCMOS
GPIO inputs*	4 x 2.5 V, 3.0 V, or 3.3 V LVTTL/LVCMOS
GPIO outputs	4 x 2.5 V LVTTL/LVCMOS
Serial (Bulk) inputs*	3 x 2.5 V, 3.0 V, or 3.3. V LVTTL/LVCMOS
Serial (Bulk) outputs	3 x 2.5 V LVTTL/LVCMOS
Camera control outputs	4 x 2.5 V LVTTL/LVCMOS

*See Table 8 on page 25.

GPIO on 12-Pin Circular Connector	
GPIO inputs	4, routed to user circuitry interface
GPIO outputs	3, routed to user circuitry interface
UART input	Routed to user circuitry interface
UART output	Routed to user circuitry interface

Frame Grabber	
Number of channels	1
Scan modes	Area Scan (Progressive) and Line Scan
Pixel depth (bits)	8, 10, 12, 14, 16, 24, and 32
Pixel clock	Minimum: 10 MHz Maximum: 120 MHz
Taps per data channel	1, 2, and 4
Image width (pixels)	Minimum: 4 and 8** Default: 640 Maximum: 16,376 Increment: 4 and 8**
Image height (pixels)	Minimum: 1 Default: 480 Maximum: 16,383 Increment: 1
Windowing/region of interest	Yes
Tap reconstruction	Interleaved only

** Image width minimum and increment are 8 pixels when **ChunkModeActive** = **True**.

Characteristics	
Operating temperature***	• 0°C to 70°C • -40°C to 85°C (industrial models only)
Storage temperature	-40°C to 85°C
Power supply	• PoE Powered: IEEE 802.3af, up to 7 Watts • External Powered: 4.8 to 16 Volts nominal
Power consumption	Less than 2 Watts when streaming at 3 Gbps

***The product is specified for operation within the stated ambient and case temperature range of its components.

Key GenICam Features

The NTx-U3 supports the seven features mandated by the USB3 Vision standard, along with many additional features. The following table lists these mandatory features, along with some of the key GenICam features. The full list of features can be seen in the Device Control dialog box of Pleora's eBUS Player application.

Table 3: Key GenICam Features

Feature	Description
Width	Specifies the width of the image (in pixels).
Height	Specifies the height of the image (in pixels).
OffsetX	Specifies the horizontal image offset (in pixels).
OffsetY	Specifies the vertical image offset (in pixels).
PixelFormat	Specifies the format of the pixel provided by the device. Available pixel formats are: • Monochrome pixel formats, 8 to 16 bits • Bayer pixel formats, 8 to 16 bits • RGB, 8 bits • BGR, 8 bits • YUV411_8_UYYVYY • YUV422_8_UYVY • YUV8_UYV • YCbCr422_8_CbYCrY • YCbCr709_411_8_CbYYCrYY • YCbCr709_422_8_CbYCrY • Truesense Sparse Color Filter Pattern, 8 to 14 bits (SCF1WGWR8, SCF1WGWR10, SCF1WGWR12, and SCF1WGWR14) **Note:** Early versions of the product will show the Truesense pixel formats as SCFWGWR8, SCFWGWR10, SCFWGWR12, and SCFWGR14.
DeviceScanType	Specifies the sensor scan type, such as Area Scan or Line Scan.
SensorDigitizationTaps	Specifies the number of digitized samples output simultaneously by the camera, 1, 2, or 4 taps.
PixelBusTimeSlotsCount	Specifies the number of pixel clocks required to transfer pixel data on the pixel bus. This feature is available for the following pixel formats: • YUV422_8_UYVY • YCbCr422_8_CbYCrY • YCbCr709_422_8_CbYCrY

Chapter 3

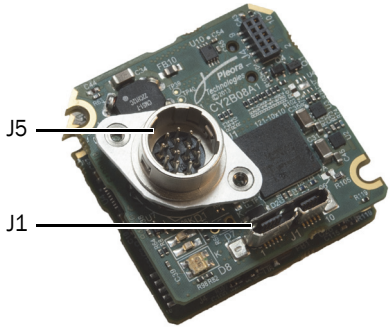
NTx-U3 Connections

This chapter describes the NTx-U3 connections, including connector details and pinout information. When the NTx-U3 is powered, you can observe the status LEDs.

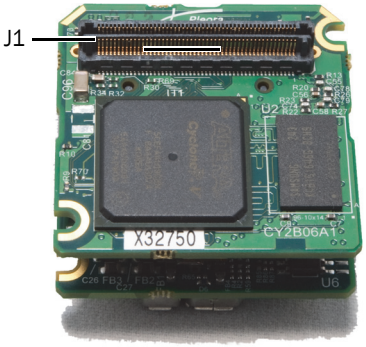
The following topics are covered in this chapter:

Connector Locations

The following images and table describe the NTx-U3 connectors.



USB PHY Board



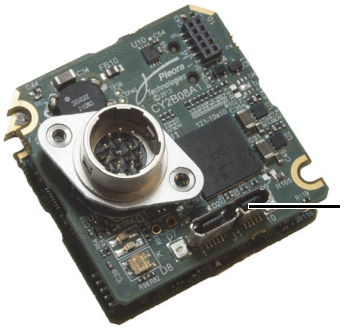
FPGA Board

Table 4: Connectors

ID	Location	Type	Description
J5	USB PHY board	12-pin circular connector	Provides external signals, such as serial communication and GPIO, to the NTx-U3. For the externally-powered models, provides power to the NTx-U3.
J1	USB PHY board	Micro-B USB 3.0 connector	Connects a computer to the NTx-U3 using a USB3 Vision connection. Compatible with USB 2.0 and 3.0 (SuperSpeed) connections. Supports power over USB 3.0 (up to 900 mA) and USB 2.0 (up to 500 mA).
J2 and J3 (not shown)	USB PHY board	60-pin connectors	Allow communication between the FPGA board and the USB PHY board. In the photographs above, the connectors are located between the boards.
J1	FPGA board	100-pin user circuitry connector	Interfaces directly to the camera head or other external device. The connector is hermaphroditic, meaning the same part is used as the header and receptacle.
J2 and J3 (not shown)	FPGA board	60-pin connectors	Allow communication between the FPGA board and the USB PHY board. In the photographs above, the connectors are located between the boards.

Micro-B USB 3.0 Connector

The NTx-U3 uses a standard vertical Micro-B USB 3.0 connector for communication with your computer. This connector is compatible with USB 2.0 and 3.0 (SuperSpeed) connections. It supports power over USB 2.0 (up to 500 mA) and over USB 3.0 (up to 900 mA).



Shield

The Micro-B USB 3.0 connector has a metal shell or shield. This shield is connected to the digital ground through a parallel capacitor and ferrite bead.

Locking Connectors

The NTx-U3 has been designed to support the Micro-B locking connectors specified by the USB3 Vision standard. If a locking connector is used, the case designed for the NTx-U3 must have threaded screw holes that comply with the connectors specified in the USB3 Vision standard. The NTx-U3 has been designed to provide the appropriate clearance around the vertical USB 3.0 connector, so that when a locking connector is attached, the screws will not damage the printed circuit board (PCB).

12-Pin Circular Connector

This section describes the GPIO, serial, and power connections for the NTx-U3.

GPIO Pinouts

The four GPIO inputs, three GPIO outputs, and two serial communication pins on the 12-pin circular connector are routed to the 100-pin user circuitry connector. The inputs and outputs can be connected to user logic, such as level translators or optocouplers, and then routed to the NTx-U3 GPIO signals.

If you plan to place optocouplers on the camera head, maximal isolation is determined by the design of the GPIO traces on the NTx-U3. The NTx-U3 uses 0.5 mm pitch connectors, resulting in 0.2 mm creepage/clearance for GPIOs. This corresponds to a 63 V isolation grade for Pollution Degree 1 (Pollution Degree 1: No pollution or only dry, non-conductive pollution occurs. The pollution has no influence).

Serial Pinouts

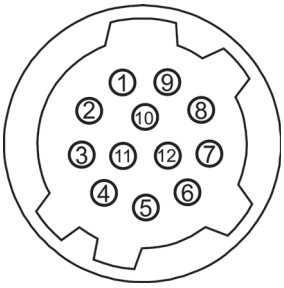
The BULK_RX, BULK_TX, and BULK_CLK signals are routed to the NTx-U3 100-pin user circuitry connector. The signals can be connected to user logic, such as an RS232 level translator, and then routed to the NTx-U3 UART TX/RX pins, USRT TX/RX/CLK pins, or I2C SDA/SCL pins. For detailed information about the pinouts, see "100-Pin User Circuitry Connector Pinouts" on page 20. For information about the UART, USRT, and I2C (Inter-Integrated Circuit) interfaces, see "Bulk Interfaces" on page 37.

The UART TX and RX signals are connected to the 12-pin circular connector through a ferrite bead, part number BLM15AG121SN1D (120 Ohms @ 100 MHz) and an 11 Ohm serial resistor. There is no logic circuit because GPIO logic must be designed on your board. These signals are protected by an ESD suppressor, part number EZJ-Z0V420WA (+/-30 V, protection up to Level 4 ESD). The operational voltage level on these signals is between -30 V and +30 V. As part of your design, you can define the direction and function for these pins.

Power Pinout

The power pin is used with the externally-powered model. The NTx-U3 supports 4.5 V to 16 V input. The circuitry of your design, along with the NTx-U3, can draw a maximum of 1.5 A.

The externally-powered model requires a maximum of 1.1 W (0.9 W typical) of external power. We recommend that you use an external power supply that can supply at least 1.3 W.



For more information about the NTx-U3 power requirements, see "Powering the NTx-U3" on page 25.

Table 5: 12-Pin Circular Connector Pinouts

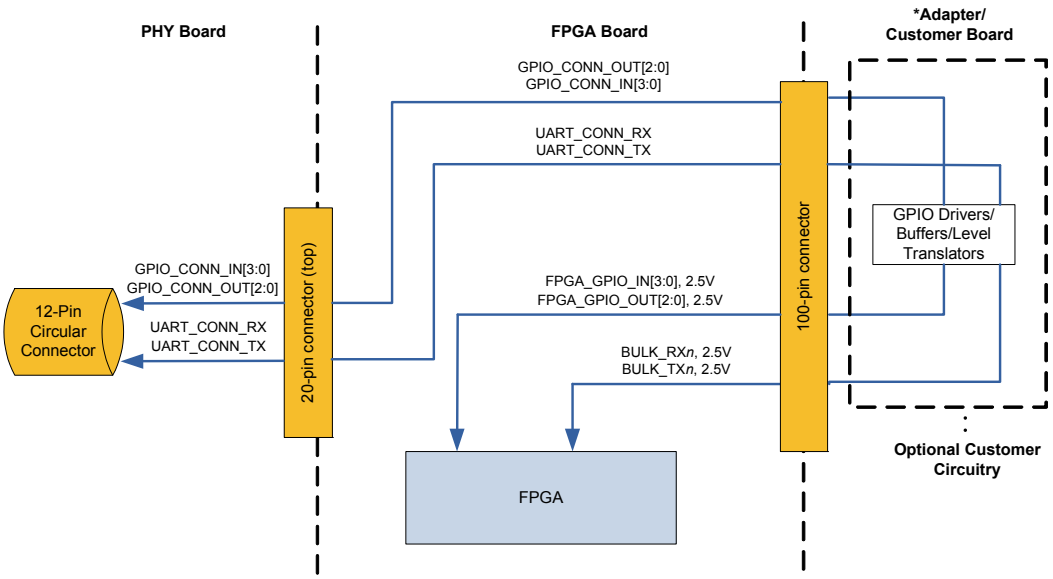
Pin	Name	Type	Notes
1	RET	Power return	Power ground
2	VIN	Power input	Protected by 600 W @ 1.0 ms PP Zener TVS, +/- 16 kV per HBM; receives 4.5 V to 16 V unfiltered DC input. 1.5 A maximum power input for the NTx-U3 and your sensor and camera electronics. Reverse voltage protection circuit up to -30 VDC.
3	GPIO_CONN_IN3	GPIO input	Protected by ESD suppressors to IEC61000-4-2, Level 4 (+/-8 kV contact, +/-15 kV air discharge). EMI filtered by ferrite bead 120 Ohm @ 100 MHz.
4	GPIO_CONN_OUT2	GPIO output	ESD/EMI information is the same as pin 3.
5	GND	Ground	Signal ground. Ferrite bead 0.2 A, 600 Ohm @ 100 MHz to DGND of USB PHY board.
6	GPIO_CONN_IN2	GPIO input	ESD/EMI information is the same as pin 3.
7	GPIO_CONN_OUT1	GPIO output	ESD/EMI information is the same as pin 3.
8	GPIO_CONN_IN1	GPIO input	ESD/EMI information is the same as pin 3.
9	GPIO_CONN_OUT0	GPIO output	ESD/EMI information is the same as pin 3.
10	GPIO_CONN_IN0	GPIO input	ESD/EMI information is the same as pin 3.
11	UART_CONN_TX	Input	ESD/EMI information is the same as pin 3. Has an 11 Ohm serial resistor.
12	UART_CONN_RX	Input	ESD/EMI information is the same as pin 3. Has an 11 Ohm serial resistor.
Shell	GND_CHASSIS	Ground	For the purpose of EMI prevention, provide good electrical contact between the connector shell and the enclosure.

GPIO Routing

The following image demonstrates the NTx-U3 GPIO routing.

Your board is responsible for making the following connections:

- Connecting **UART_CONN_TX** and **UART_CONN_RX** to **BULK_TX**n and **BULK_RX**n.
- Connecting **GPIO_CONN_OUT**[**2:0**] to **FPGA_GPIO_OUT**[**2:0**].
- Connecting **GPIO_CONN_IN**[**3:0**] to **FPGA_GPIO_IN**[**3:0**].



*An example of an adapter board is the NTx-Mini adapter board. If you are using the NTx-Mini adapter board, keep in mind the following notes:

- **UART_CONN_TX** and **UART_CONN_RX** are not connected to **BULK_RX**n and **BULK_TX**n, and cannot be used.
- For the **BULK_RX**n and **BULK_TX**n signals, *n* can be 0, 1, or 2.
- **GPIO_CONN_IN**[**3:0**] is connected to **FPGA_GPIO_IN**[**3:0**] through 33 Ohm resistors.
- **GPIO_CONN_OUT**[2:0] is connected to **FPGA_GPIO_OUT**[2:0] through 33 Ohm resistors.

Mapping the 12-Pin Circular Connector to the 100-Pin User Circuitry Connector

This section describes how the pins of the 12-pin circular connector are directly routed to the 100-pin user circuitry connector on the NTx-U3 FPGA board. The use for each pin listed below is a suggestion, as you can choose to use the pin for other functions.

Table 6: 12-Pin Circular Connector to 100-Pin User Circuitry Connector Mapping

Name	Pin on the 12-pin circular connector — USB PHY board	Pin on the 100-pin user circuitry connector — FPGA board
GPIO_CONN_IN3	3	17
GPIO_CONN_OUT2	4	16
GPIO_CONN_IN2	6	15
GPIO_CONN_OUT1	7	14
GPIO_CONN_IN1	8	13
GPIO_CONN_OUT0	9	12
GPIO_CONN_IN0	10	11
UART_CONN_TX	11	20
UART_CONN_RX	12	19

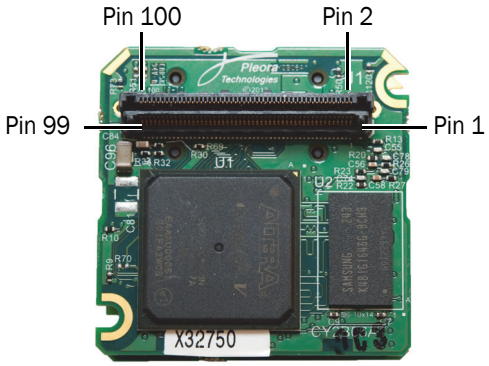
All of the signals in the table above are connected with the 12-pin circular connector through a ferrite bead (120 Ohms @ 100 MHz). UART pins also have serial 11 Ohm resistors. There is no logic circuit because the GPIO logic must be designed on your board. These signals are all protected by ESD suppressors (EZJ-Z0V420WA, +/-30 V, protection up to Level 4 ESD). The operational voltage level on these signals is between -30 V and +30 V. As part of your design, you can define the direction and function for these pins.

12-Pin Circular Connector Mate

The mating connector for the 12-pin circular connector is a Hirose 12-pin connector, part number HR10A-10P-12S(73).

100-Pin User Circuitry Connector Pinouts

The following table provides the pinouts for the 100-pin user circuitry connector.



All user circuitry inputs are 2.5 V LVTTL.

For a mapping of PLC signals, see "Signal Handling" on page 59. For a mapping of pins on the 12-pin circular connector and the 100-pin user circuitry connector, see "Mapping the 12-Pin Circular Connector to the 100-Pin User Circuitry Connector" on page 19.

Table 7: 100-Pin User Circuitry Pinouts

Pin	Name	Type	Description
1	VCC_5V_30V	PWR OUT	VIN or VBUS. For more information, see "Powering the NTx-U3" on page 25. For the USB-powered models, do not use VBUS to power your camera. Instead, you must use the 3.3 V power output. If you need more than 3.3 V @ 0.5 A, use the externally-powered NTx-U3, which allows you to power your camera using VIN or 3.3 V, or both.
2	VCC_5V_30V	PWR OUT	VIN or VBUS. For more information, see "Powering the NTx-U3" on page 25. For the USB-powered models, do not use VBUS to power your camera. Instead, you must use the 3.3 V power output. If you need more than 3.3 V @ 0.5 A, use the externally-powered NTx-U3, which allows you to power your camera using VIN or 3.3 V, or both.
3	RET	RET (GND)	RET or GND. For more information, see "Powering the NTx-U3" on page 25.
4	RET	RET (GND)	RET or GND. For more information, see "Powering the NTx-U3" on page 25.

Table 7: 100-Pin User Circuitry Pinouts (Continued)

Pin	Name	Type	Description
5	+2.5 V	PWR OUT	2.5 V output. Can supply up to 0.1 A. See **warning in table note 1**.
6	+3.3 V	PWR OUT	3.3 V output. Can supply up to 0.5 A, if powered through the USB port, and up to 1.5 A if powered through the external power supply.
7	+2.5 V	PWR OUT	2.5 V output. Can supply up to 0.1 A. See **warning in table note 1**.
8	+3.3 V	PWR OUT	3.3 V output. Can supply up to 0.5 A. Can supply up to 0.5 A, if powered through the USB port, and up to 1.5 A if powered through the external power supply.
9	N.C.	N.C.	Not connected.
10	N.C.	N.C.	Not connected.
11	GPIO_CONN_IN0*	IN	To pin 10 of 12-pin circular connector. See table note 4.
12	GPIO_CONN_OUT0*	OUT	To pin 9 of 12-pin circular connector. See table note 4.
13	GPIO_CONN_IN1*	IN	To pin 8 of 12-pin circular connector. See table note 4.
14	GPIO_CONN_OUT1*	OUT	To pin 7 of 12-pin circular connector. See table note 4.
15	GPIO_CONN_IN2*	IN	To pin 6 of 12-pin circular connector. See table note 4.
16	GPIO_CONN_OUT2*	OUT	To pin 4 of 12-pin circular connector. See table note 4.
17	GPIO_CONN_IN3*	IN	To pin 3 of 12-pin circular connector. See table note 4.
18	N.C.	N.C.	Not connected.
19	UART_CONN_RX*	IN	To pin 12 of 12-pin circular connector. See table note 4.
20	UART_CONN_TX*	OUT	To pin 11 of 12-pin circular connector. See table note 4.
21	GND	GND	
22	GND	GND	
23	PWR_ON_RSTN	INOUT, OC	Power on Reset. See table note 2.
24	BULK_TX0*	OUT	Bulk interface 0 UART and USRT output.
25	N.C	N.C	Not connected.
26	BULK_RX0*	IN	Bulk interface 0 UART and USRT input. See table note 4. **See warning in table note 5.**
27	FPGA_GPIO_IN0*	IN	Connected to the Programmable Logic Controller (PLC). See table note 4. **See warning in table note 5.**
28	BULK_CLK0*	OUT	Bulk interface 0 USRT output clock.
29	FPGA_GPIO_IN1*	IN	Connected to the PLC. See table note 4. **See warning in table note 5.**
30	BULK_TX1*	OUT	Bulk interface 1 UART and USRT output, or I2C serial data line (SDA).

Table 7: 100-Pin User Circuitry Pinouts (Continued)

Pin	Name	Type	Description
31	FPGA_GPIO_IN2*	IN	Connected to the PLC. See table note 4. **See warning in table note 5.**
32	BULK_RX1*	IN	Bulk interface 1 UART and USRT input. **See warning in table note 5.**
33	FPGA_GPIO_IN3*	IN	Connected to the PLC. See table note 4. **See warning in table note 5.**
34	BULK_CLK1*	OUT	Bulk interface 1 USRT output clock or I2C serial clock line (SCL).
35	FPGA_GPIO_OUT0*	OUT	Connected to the PLC.
36	BULK_TX2*	OUT	Bulk interface 2 UART and USRT output.
37	FPGA_GPIO_OUT1*	OUT	Connected to the PLC.
38	BULK_RX2*	IN	Bulk interface 2 UART and USRT input. See table note 4. **See warning in table note 5.**
39	FPGA_GPIO_OUT2*	OUT	Connected to the PLC.
40	BULK_CLK2*	OUT	Bulk interface 2 USRT clock.
41	FPGA_GPIO_OUT3*	N.C	Reserved GPIO.
42	GND	GND	
43	FPGA_SEL*	INOUT OC/N.C	Selection of FPGA load. See table note 3. This signal has been added to ensure consistency with earlier Pleora products, such as the iPORT NTx-Mini Embedded Video Interface. For newer products, leave it N.C.
44	PB0_CLK*	IN	Pixel bus clock. **See warning in table note 5.**
45	GND	GND	
46	PB0_CLK_IN*	IN	For future use. Connect to ground.
47	PB0_DATA0*	IN	Pixel bus data 0. See table note 4. **See warning in table note 5.**
48	GND	GND	
49	PB0_DATA1*	IN	Pixel bus data 1. See table note 4. **See warning in table note 5.**
50	PB0_DATA8*	IN	Pixel bus data 8. See table note 4. **See warning in table note 5.**
51	PB0_GND*	GND	
52	PB0_DATA9*	IN	Pixel bus data 9. See table note 4. **See warning in table note 5.**
53	PB0_DATA2*	IN	Pixel bus data 2. See table note 4. **See warning in table note 5.**
54	GND	GND	
55	PB0_DATA3*	IN	Pixel bus data 3. See table note 4. **See warning in table note 5.**
56	PB0_DATA10*	IN	Pixel bus data 10. See table note 4. **See warning in table note 5.**
57	GND	GND	

Table 7: 100-Pin User Circuitry Pinouts (Continued)

Pin	Name	Type	Description
58	PB0_DATA11*	IN	Pixel bus data 11. See table note 4. **See warning in table note 5.**
59	PB0_DATA4*	IN	Pixel bus data 4. See table note 4. **See warning in table note 5.**
60	GND	GND	
61	PB0_DATA5*	IN	Pixel bus data 5. See table note 4. **See warning in table note 5.**
62	PB0_DATA12*	IN	Pixel bus data 12. See table note 4. **See warning in table note 5.**
63	PB0_CTRL_OUT0*	OUT	Connected to the PLC.
64	PB0_DATA13*	IN	Pixel bus data 13. See table note 4. **See warning in table note 5.**
65	PB0_DATA6*	IN	Pixel bus data 6. See table note 4. **See warning in table note 5.**
66	PB0_CTRL_OUT1*	OUT	Connected to the PLC.
67	PB0_DATA7*	IN	Pixel bus data 7. See table note 4. **See warning in table note 5.**
68	PB0_DATA14*	IN	Pixel bus data 14. See table note 4. **See warning in table note 5.**
69	GND	GND	
70	PB0_DATA15*	IN	Pixel bus data 15. See table note 4. **See warning in table note 5.**
71	PB0_DATA16*	IN	Pixel bus data 16. See table note 4. **See warning in table note 5.**
72	GND	GND	
73	PB0_DATA17*	IN	Pixel bus data 17. See table note 4. **See warning in table note 5.**
74	PB0_DATA24*	IN	Pixel bus data 24. See table note 4. **See warning in table note 5.**
75	PB0_FVAL*	IN	Pixel bus frame valid. **See warning in table note 5.**
76	PB0_DATA25*	IN	Pixel bus data 25. See table note 4. **See warning in table note 5.**
77	PB0_DATA18*	IN	Pixel bus data 18. See table note 4. **See warning in table note 5.**
78	PB0_DVAL*	IN	Pixel bus data valid. **See warning in table note 5.**
79	PB0_DATA19*	IN	Pixel bus data 19. See table note 4. **See warning in table note 5.**
80	PB0_DATA26*	IN	Pixel bus data 26. See table note 4. **See warning in table note 5.**
81	GND	GND	
82	PB0_DATA27*	IN	Pixel bus data 27. See table note 4. **See warning in table note 5.**
83	PB0_DATA20*	IN	Pixel bus data 20. See table note 4. **See warning in table note 5.**
84	GND	GND	
85	PB0_DATA21*	IN	Pixel bus data 21. See table note 4. **See warning in table note 5.**
86	PB0_DATA28*	IN	Pixel bus data 28. See table note 4. **See warning in table note 5.**
87	PB0_MVAL*	IN	Pixel bus chunk data valid. **See warning in table note 5.**
88	PB0_DATA29*	IN	Pixel bus data 29. See table note 4. **See warning in table note 5.**
89	PB0_DATA22*	IN	Pixel bus data 22. See table note 4. **See warning in table note 5.**

Table 7: 100-Pin User Circuitry Pinouts (Continued)

Pin	Name	Type	Description
90	PB0_LVAL*	IN	Pixel bus line valid. **See warning in table note 5.**
91	PB0_DATA23*	IN	Pixel bus data 23. See table note 4. **See warning in table note 5.**
92	PB0_DATA30*	IN	Pixel bus data 30. See table note 4. **See warning in table note 5.**
93	GND	GND	
94	PB0_DATA31*	IN	Pixel bus data 31. See table note 4. **See warning in table note 5.**
95	PB0_CTRL_OUT2*/ 33.3 MHz	OUT	Connected to the PLC. The behavior of this pin is configurable using eBUS Player (or an application created using the eBUS SDK) using the **PixelBusCameraControl2FunctionSelect** GenICam feature. Set **PixelBusCameraControl2FunctionSelect** to either **PlcPb0CC2** (to use the pin for camera control) or **SingleEndedClock_33p3MHz** (to use the pin as a single-ended 33.3 MHz clock). By default, this pin is used for camera control.
96	GND	GND	
97	PB0_CTRL_OUT3*/ GND	OUT	Connected to the PLC. If pin 95 is used for camera control, this pin is also used for camera control (**PlcPb0CC3**). If pin 95 is configured as a 33.3 MHz clock, this pin is **GND**.
98	N.C.	N.C.	Not connected.
99	GND	GND	
100	GND	GND	

* See Table 8 on page 25.

1. Because the 2.5 V power switch is powered from the USB port in both the USB and externally-powered models, drawing more than 100 mA from the 2.5 V pins (USB 3.0) or drawing any current from the 2.5 V pins (USB 2.0) can cause continuous power cycling.
2. **PWR_ON_RSTN** is a bidirectional open collector pin with a 10 KOhm resistor to 3.3 V on the FPGA board. This signal is high when power on the NTx-U3 is at the appropriate levels. You can do any of the following:
   - Leave the pin set to N.C.
   - Connect the signal to the power ready signal of the user circuitry.
   - Use the signal to start the configuration of user devices, such as FPGAs or CPUs.
   - Use the signal to initiate a reset of the FPGA.

3. **FPGA_SEL** selects the FPGA load to be used. When this pin is set to high (1), the main load is used. When this pin is set to low (0), the backup load is used. The FPGA board provides a 1KOhm pull-up to 2.5 V and a DIP switch to GND (normally off). You can:
   - Leave this pin set to N.C. (recommended).
   - Monitor the load that is used.
   - Apply the backup load by setting the DIP switch to GND or by using an open-collector signal.
4. If you do not use any of these pins, we recommend that you tie them to GND instead of leaving them not connected.
5. **IMPORTANT:** If your electronics output 3.0 V or 3.3 V, place a 33 Ohm serial resistor between the following inputs on the 100-pin user circuitry connector and your electronics to avoid damage to the FPGA: PB0_DATA*n*, PB0_CLK, PB0_FVAL, PB0_LVAL, PB0_MVAL, PB0_DVAL, BULK_RX*n*, and FPGA_GPIO_IN*n*.

Table 8: Input/Output Levels on the User Circuitry Interface

Input/output level	Rating
VOH	2 V minimum
VOL	0.4 V maximum
VIH	1.7 V minimum 3.6 V maximum
VIL	0.7 V maximum -0.3 V minimum

Powering the NTx-U3

Depending on your requirements, you can purchase a USB-powered version of the NTx-U3, or a version that is powered externally through the 12-pin circular connector.

The NTx-U3 always draws some power from the USB port. The externally-powered version draws a small amount of power for the USB controller on the NTx-U3. All power routed to the user circuitry connector is provided by the 12-pin circular connector power pin.

The USB-powered version does not receive any external power through the 12-pin circular connector power pin. All power routed to the user circuitry connector is provided through the USB port.

USB-Powered Models

As mentioned in the note above, the USB-powered NTx-U3 receives power only through the USB port. The NTx-U3 specifies its power requirements during enumeration as 900 mA for USB 3.0 and 500 mA for USB 2.0. The NTx-U3 consumes some of this power, leaving the remaining power available for other devices, such as the camera head.

Power Sequence for USB-Powered Models

When the USB interface is connected to a cable and a host computer, the USB controller starts, followed by the USB enumeration and power request process. Requests to the host computer for 900 mA or 500 mA are performed when USB 3.0 or USB 2.0 host computers are connected, respectively. During this period, the host computer can supply either 150 mA (for USB 3.0) or 100 mA (for USB 2.0), so the power regulators on the FPGA board are temporarily disabled. This also limits the supply current on the 2.5 V pins on the user circuitry connector to 100 mA (for USB 3.0) and 0 mA (for USB 2.0). Using more current from the 2.5 V pins on the 100-pin user circuitry connector during the power request process can cause the NTx-U3 to power cycle continuously. If the request is accepted by the computer, the power regulator is enabled and the FPGA board receives power, as does user circuitry connected to the 3.3 V power pin of the 100-pin user circuitry connector.

The power sequence for the USB-powered models is as follows:

1. When the USB cable is first connected: 2.5 V @ 0.1 A is available on the NTx-U3 100-pin user circuitry connector.
2. When the request is accepted, 3.3 V @ 0.5 A is available on the 100-pin user circuitry connector.

We recommend that you power the camera using 3.3 V or an external power supply, and that you do not power the camera using VBUS.

Externally-Powered Models

In the externally-powered version of the NTx-U3, the FPGA board and user circuitry are powered from the 12-pin circular connector. The USB controller on the USB PHY board is powered by the USB port.

Power Sequence for Externally-Powered Models

Ensure there is power available on the 12-pin circular connector. Otherwise, the NTx-U3 will not power up correctly.

When the USB interface is connected to a cable and a host computer, the USB controller starts and the USB enumeration and power request process begins. During this period, the computer can supply only 150 mA (for USB 3.0) or 100 mA (for USB 2.0), so the power regulators on the FPGA board are temporarily disabled. This also limits the supply current on the 2.5 V pins on the 100-pin user circuitry connector to 100 mA (for USB 3.0) and 0 mA for (USB 2.0). Using more current from the 2.5 V pins on the 100-pin user circuitry connector during the power request process can cause the NTx-U3 to power cycle continuously. When the process is complete, the power regulator is enabled and the FPGA board receives power.

The power sequence for the externally-powered models is as follows:

1. When external power is applied, it is available on the VIN pins of the 100-pin user circuitry connector.
2. When the USB cable is first connected, 2.5 V @ 0.1 A is available on the 100-pin user circuitry connector.
3. When the request is accepted, 3.3 V @ 1.5 A is available on the 100-pin user circuitry connector.

Power Consumption

The following table outlines the power consumption of the NTx-U3.

The following table lists typical values measured during characterization at room temperature, but are not guaranteed.

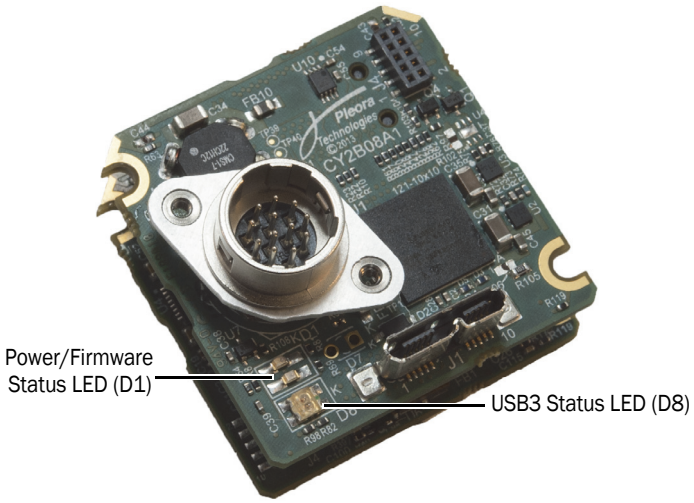
Table 9: Typical Power Consumption At Room Temperature

Power supply source	Streaming rate	Power (watts)		
		USB*	External*	Total
USB-powered	Idle	1.626	0	1.626
	800 Mbps	1.727	0	1.727
	1600 Mbps	1.793	0	1.793
	2400 Mbps	1.862	0	1.862
External-powered @ 5 V	Idle	0.649	0.985	1.634
	800 Mbps	0.725	1.007	1.733
	1600 Mbps	0.774	1.027	1.801
	2400 Mbps	0.813	1.046	1.859
External-powered @ 12 V	Idle	0.649	1.409	2.058
	800 Mbps	0.725	1.409	2.134
	1600 Mbps	0.774	1.447	2.221
	2400 Mbps	0.813	1.459	2.272

*USB refers to power consumed through the USB connector. External refers to power consumed through the 12-pin circular connector.

Status LEDs

The status LEDs indicate the operating status of the NTx-U3's USB connection and firmware. The following figure and table describe the status LEDs.



USB PHY Board

Table 10: Status LEDs

LED	ID	Description
Power/Firmware	D1	**Off.** FPGA is not configured. **Green.** Power is supplied and the FPGA is configured. **Yellow.** The backup load is running.
USB3		**Yellow (flashing quickly).** The NTx-U3 is operating properly. **Yellow (flashing).** Indicates GenCP traffic between the NTx-U3 and the host. **Green (solid).** A SuperSpeed (USB 3.0) connection is established. **Off.** A USB 2.0 connection is established.

Chapter 4

NTx-Mini Adapter Board Pinout Mapping

This section describes how the signals from the FPGA board are directly routed to the 60-pin FFC connector on the NTx-Mini adapter board. This board is intended to help you evaluate the NTx-U3 with an existing camera connected to an iPORT NTx-Mini Embedded Video Interface.

Table 11: 60-Pin FFC Connector to FPGA Board

Signal on FPGA board	NTx-Mini 60-pin connector	
Name	Pin	Name
	1	Not connected (See table note 1)
	2	Not connected
VIN	3	CAMERA_VIN
VIN	4	CAMERA_VIN
FPGA_SEL0	5	FPGA_SEL0
N.C (See table notes 2 and 3)	6	FPGA_SEL1
PWR_ON_RST	7	PWR_ON_RST#
GND	8	GND
PB0_DATA0 (See table note 2)	9	PIXEL_DATA0
PB0_DATA1 (See table note 2)	10	PIXEL_DATA1
PB0_DATA2 (See table note 2)	11	PIXEL_DATA2
PB0_DATA3 (See table note 2)	12	PIXEL_DATA3
PB0_DATA4 (See table note 2)	13	PIXEL_DATA4
PB0_DATA5 (See table note 2)	14	PIXEL_DATA5
PB0_DATA6 (See table note 2)	15	PIXEL_DATA6
PB0_DATA7 (See table note 2)	16	PIXEL_DATA7
PB0_DATA8 (See table note 2)	17	PIXEL_DATA8

Table 11: 60-Pin FFC Connector to FPGA Board (Continued)

Signal on FPGA board	NTx-Mini 60-pin connector	
Name	**Pin**	**Name**
PB0_DATA9 (See table note 2)	18	PIXEL_DATA9
GND	19	GND
PB0_DATA10 (See table note 2)	20	PIXEL_DATA10
PB0_DATA11 (See table note 2)	21	PIXEL_DATA11
PB0_DATA12 (See table note 2)	22	PIXEL_DATA12
PB0_DATA13 (See table note 2)	23	PIXEL_DATA13
PB0_DATA14 (See table note 2)	24	PIXEL_DATA14
PB0_DATA15 (See table note 2)	25	PIXEL_DATA15
PB0_DATA16 (See table note 2)	26	PIXEL_DATA16
PB0_DATA17 (See table note 2)	27	PIXEL_DATA17
PB0_DATA18 (See table note 2)	28	PIXEL_DATA18
PB0_DATA19 (See table note 2)	29	PIXEL_DATA19
GND	30	GND
PB0_DATA20 (See table note 2)	31	PIXEL_DATA20
PB0_DATA21 (See table note 2)	32	PIXEL_DATA21
PB0_DATA22 (See table note 2)	33	PIXEL_DATA22
PB0_DATA23 (See table note 2)	34	PIXEL_DATA23
PB0_MVAL (See table note 2)	35	SPARE
PB0_LVAL (See table note 2)	36	LVAL
PB0_FVAL (See table note 2)	37	FVAL
PB0_DVAL (See table note 2)	38	DVAL
BULK_RX2 (See table note 2)	39	SERTTFG
BULK_TX2 (See table note 2)	40	SERTC
GND	41	GND
PB0_CTRL_OUT0 (See table note 2)	42	CC1
PB0_CTRL_OUT1 (See table note 2)	43	CC2
PB0_CTRL_OUT2 (See table note 2)	44	CC3
PB0_CTRL_OUT3 (See table note 2)	45	CC4
BULK_RX0 (See table note 2)	46	BULK0_RXD
BULK_TX0 (See table note 2)	47	BULK0_TXD
BULK_CLK0 (See table note 2)	48	BULK0_CLK

Table 11: 60-Pin FFC Connector to FPGA Board (Continued)

Signal on FPGA board	NTx-Mini 60-pin connector	
Name	Pin	Name
BULK_RX1 (See table note 2)	49	UART1_RXD
BULK_TX1 (See table note 2)	50	UART1_TXD
PB0_DATA24 (See table note 2)	51	Reserved
GND	52	GND
PB0_DATA25 (See table note 2)	53	Reserved
PB0_DATA26 (See table note 2)	54	Reserved
PB0_DATA29	55	Reserved
PB0_DATA28	56	OUT_CLK0
PB0_CLK (See table note 2)	57	PIXEL_CLK
Reserved	58	Reserved
PB0_DATA30 (See table note 2)	59	Reserved
PB0_DATA31 (See table note 2)	60	Reserved

Table Notes:

1. If you require 2.5 V to power the camera, you can install a 0 Ohm 0805 resistor at R17 on the NTx-Mini adapter board (shown below), and power the camera using pin 1. This pin can supply a maximum of 0.25 A at 2.5 V.
2. These signals are connected to the FPGA board through 33 R resistors.
3. To test a 32-bit wide pixel bus, you can do the following:

   a. On the adapter board, wire pin 26 on the J3 connector (30-pin) (which is not populated) to either of these pins.

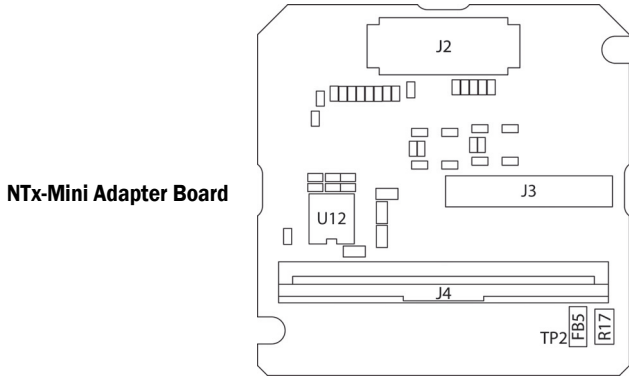
   - Pin 6 on the J4 connector (60-pin).

   - Or -

   - Test point TP2 (which is connected to pin 6 on the J4 connector).

   b. Connect **PB0_DATA27** from the camera to pin 6 of the 60 pin connector.

Figure 2: NTx-Mini Adapter Board



Chapter 5

Ambient and Junction Temperatures

This chapter provides you with the information you need to ensure the optimal operating temperature for your NTx-U3.

You should store the NTx-U3 at temperatures between -40°C to +85°C.

The tables in this chapter list the components that consume the largest amount of power on the NTx-U3, and that will therefore be most affected by high temperatures. If you are designing a product to operate at (or above) 85° C, you must provide a method to cool these components using a heat sink or thermal pad.

Thermal Guidelines, Standard Models

Table 12: Thermal Guidelines, Standard Models

Reference designator	Location	Component and manufacturer part number	Rating for component on standard Pleora product*
U1	USB PHY board	Cypress FX3 USB controller **Part number:** CYUSB3014-BZXC	**Ambient:** 0°C to +70°C **Junction:** Not specified **Case:** Not specified **Junction-to-case thermal resistance ΘJC:** Not specified **Junction-to-ambient thermal resistance ΘJA:** Not specified **Power consumption:** ~450 mW

Table 12: Thermal Guidelines, Standard Models (Continued)

Reference designator	Location	Component and manufacturer part number	Rating for component on standard Pleora product*
U2	FPGA board	Samsung DDR3 **Part number:** K4B1G1646G-BCH9000	**Ambient:** Not specified **Junction:** Not specified **Case:** 0°C to +95°C **Junction-to-case thermal resistance ΘJC:** Not specified **Junction-to-ambient thermal resistance ΘJA:** Not specified **Power consumption:** ~ 200 mW
U1	FPGA board	Altera FPGA **Part number:** 5CEFA4U19C8N	**Ambient:** Not specified **Junction:** 0° to +85°C **Case:** Not specified **Junction-to-case thermal resistance ΘJC:** 5 (°C/W) **Junction-to-ambient thermal resistance ΘJA:** • **Still air:** 23.6 (°C/W) • **100 ft./min:** 19.5 (°C/W) • **200 ft./min:** 17.5 (°C/W) • **400 ft./min:** 15.9 (°C/W) **Power consumption:** ~ 850 mW

* ΘJC = (Tj - Ta)/Ptop, where Ptop = Power dissipation from the top of the package.

ΘJA = (Tc - Ta)/P, where P = Total power dissipation.

Thermal Guidelines, Industrial Models

Table 13: Thermal Guidelines, Industrial Models

Reference designator	Location	Component and manufacturer part number	Rating for component on standard Pleora product*
U1	USB PHY board	Cypress FX3 USB controller **Part number:** CYUSB3014-BZXI	**Ambient:** -40°C to +85°C **Junction:** Not specified **Case:** Not specified **Junction-to-case thermal resistance ΘJC:** Not specified **Junction-to-ambient thermal resistance ΘJA:** Not specified **Power consumption:** ~450 mW

Table 13: Thermal Guidelines, Industrial Models (Continued)

Reference designator	Location	Component and manufacturer part number	Rating for component on standard Pleora product*
U2	FPGA board	ISSI DDR3 **Part number:** IS43TR16640A-15GBLI	**Ambient:** Not specified **Junction:** Not specified **Case:** -40°C to +95°C **Junction-to-case thermal resistance ΘJC:** Not specified **Junction-to-ambient thermal resistance ΘJA:** Not specified **Power consumption:** ~ 200 mW
U1	FPGA board	Altera FPGA **Part number:** 5CEFA4U19I7N	**Ambient:** Not specified **Junction:** -40°C to +100°C **Case:** Not specified **Junction-to-case thermal resistance ΘJC:** 5 (°C/W) **Junction-to-ambient thermal resistance ΘJA:** • **Still air:** 23.6 (° C/W) • **100 ft./min:** 19.5 (°C/W) • **200 ft./min:** 17.5 (°C/W) • **400 ft./min:** 15.9 (°C/W) **Power consumption:** ~ 850 mW

* ΘJC = (Tj - Ta)/Ptop, where Ptop = Power dissipation from the top of the package.

ΘJA = (Tc - Ta)/P, where P = Total power dissipation.

Chapter 6

Bulk Interfaces

This chapter describes the bulk interfaces available on the NTx-U3, and the supported protocols.

The following topics are covered in this chapter:

Bulk Interfaces and Supported Protocols

The NTx-U3 has three Bulk interface ports available for serial communication.

Each port supports the standard UART (Universal Asynchronous Receiver/Transmitter) and USRT (Universal Synchronous Receiver/Transmitter) protocol. Alternatively, you can use the Bulk1 port for I2C (Inter-Integrated Circuit). The Bulk interfaces are 2.5 V.

The Bulk interface ports are available on the 100-pin user circuitry connector, as outlined in the following table.

Table 14: Bulk Interface and Connector Pinouts

		Bulk mode		
Pin	**Bulk signal name**	**UART**	**USRT [1, 2]**	**I2C**
24	BULK_TX0	TXD	TXD	
26	BULK_RX0	RXD	RXD	
28	BULK_CLK0		SCK	
30	BULK_TX1	TXD	TXD	SDA
32	BULK_RX1	RXD	RXD	
34	BULK_CLK1		SCK	SCL
36	BULK_TX2	TXD	TXD	
38	BULK_RX2	RXD	RXD	
40	BULK_CLK2		SCK	

UART Signals

The standard serial port communication uses the following signals:

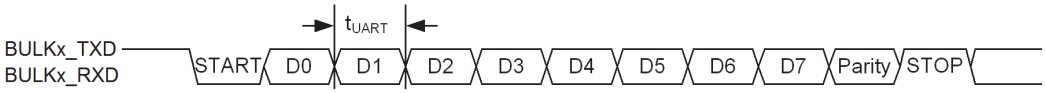
- BULK_TXD*n*
- BULK_RXD*n*
- BULK_CLK*n,* which is used to maintain synchronization between the receiver/transmitter
- DGND (return)

Where *n* is 0, 1, or 2.

UART Timing

The UART interface supports:

- 8-bit data transfer
- 1 start bit
- Programmable stop bit(s): 1 or 2
- Parity: Even, odd, or none
- Baud rates:
  - Predefined rates: 9600, 14 400, 19 200, 28 800, 38 400, 57 600, 115 200
  - Programmable
- Loop back mode from downstream to upstream



A number of preset baud rates can be used. If you require a baud rate that is not covered by the presets, you can specify your own baud rate. To specify your own baud rate:

1. In the **Device Control** dialog box, under **Port Communication**, choose **Programmable** in the **BulkBaudRate** list.
2. In the **BulkBaudRateFactor** field, enter a baud rate between 1 and 511.

The NTx-U3 calculates the baud rate using the following equation:
(66.666666 MHz * 1000000)/(BulkBaudRateFactor * 16)

Table 15: UART Baud Rates

Baud rate (BR) [bps]	Notes
9,600	Preset 0 (default)
14,400	Preset 1
19,200	Preset 2

Table 15: UART Baud Rates (Continued)

Baud rate (BR) [bps]	Notes
28,800	Preset 3
38,400	Preset 4
57,600	Preset 5
115,200	Preset 6
Maximum (when BulkBaudRateFactor is set to 1): 4,166,667 **Minimum (when BulkBaudRateFactor is set to 511):** 8,154	Programmable baud rate

The following table lists the A.C. operating characteristics of the UART interface.

Table 16: A.C. Operating Characteristics of the UART Interface

Parameter	Symbol	Minimum	Maximum	Units
Data period	t^{UART}	0.240	122.64	µs
Baud rate	BR	8,154	4,166,667	bps

USRT Signals

The USRT (Universal Synchronous Receiver/Transmitter) serial interface resembles the UART interface, but adds a clock signal to enable synchronous communication.

Table 17: USRT Signal Nomenclature

Signal	Generic signal
BULK_RXD*n*	RXD
BULK_TXD*n*	TXD
BULK_CLK*n*	SCK

Where *n* is 0, 1, or 2.

USRT Timing

The following table lists the supported USRT clock frequencies and periods.

Table 18: Supported USRT Clock Frequencies and Periods

Bulk system clock divider	Clock period, tSCK (ns)	Clock frequency (MHz)*
By 2	60	16.667
By 4	120	8.333
By 8	240	4.167
By 16	480	2.083
By 32	960	1.042
By 64	1920	0.521
By 128	3840	0.260
By 256	7680	0.130

* To obtain the exact frequency, divide the 33.333 MHz clock speed by one of: 2, 4, 8, 16, 32, 64, 128, or 256.

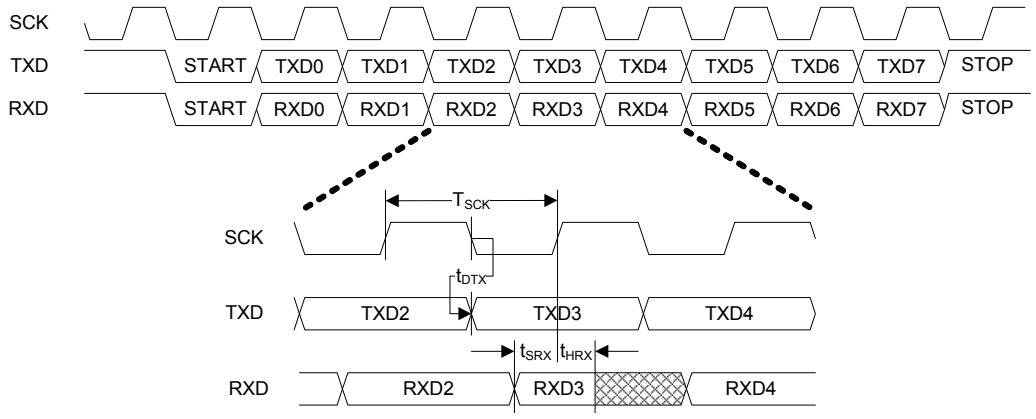


Table 19: USRT Delays

Delay	Minimum	Maximum
SCK to TXD delay t_{DTx}	-12 ns	12 ns
RXD setup time t_{SRx}	22 ns	N/A
RXD hold time t_{HRx}	0 ns	N/A

I2C Signals

An I2C master mode is available that can be used to communicate with I2C slave devices. The I2C interface is a two-wire, bi-directional serial bus with a serial clock line (SCL) and a serial data line (SDA). Note that all devices connected to these signals must have open drain or open collector outputs. Both lines must be pulled up to VCC by external resisters.

I2C is available in version 1.2 (and later) of the NTx-U3.

Table 20: I2C Signal Nomenclature

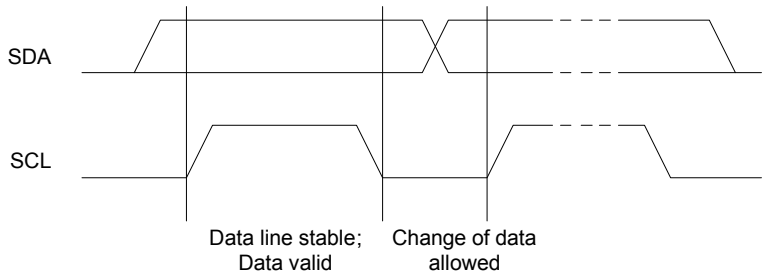
Signal	Generic signal
BULK_RXD1	Not used
BULK_TXD1	SDA
BULK_CLK1	SCL

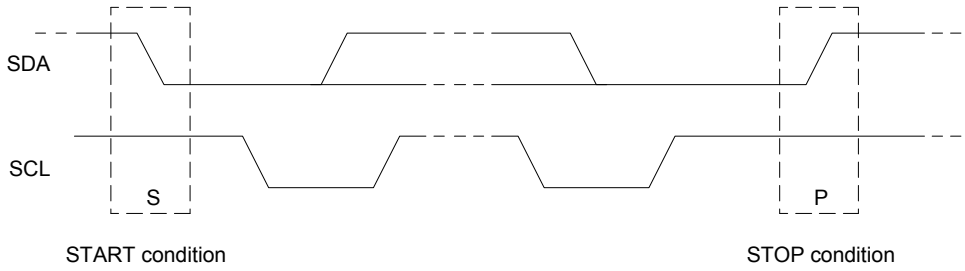
I2C Transmission Speeds

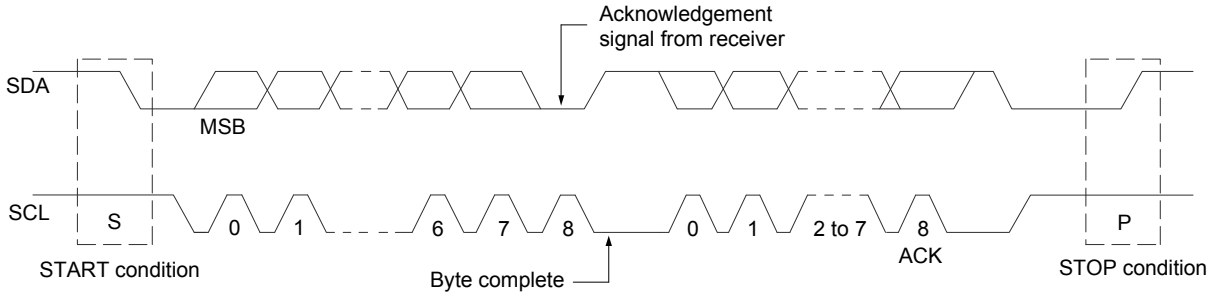
The NTx-U3 is compatible with the Philips I2C standard and support the following transmission speeds:

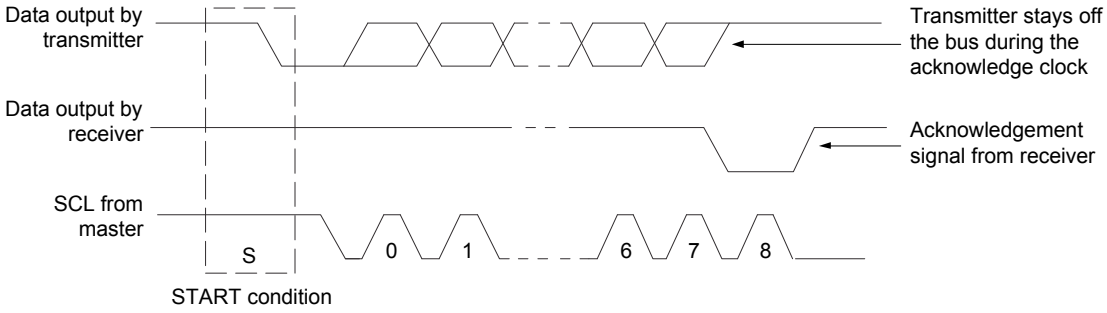
- **Normal.** 100 kbit/s
- **Fast.** 400 kbit/s

Data is transferred synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is an SCL clock pulse for each data bit with the most significant bit (MSB) being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL.









GenICam Interface for Serial Communication Configuration

The following GenICam features are available for serial communication configuration.

Table 21: GenICam Features Available for Serial Communication

Feature	Description
BulkSelector	Selects Bulk0, Bulk1, or Bulk2 for configuration.
BulkMode	UART/USRT/I2C protocol. Please note that I2C is available when BulkSelector = Bulk1.
BulkSystemClockDivider	Defines the frequency of the USRT output clock. The actual frequency produced is equal to the system clock frequency divided by the factor set by this feature. Available dividers are 2, 4, 8, 16, 32, 64, 128, and 256.
BulkOutputClockFrequency	Represents the frequency of the USRT output clock controlled by the **BulkSystemClockDivider**. The frequency is calculated using the following equation: $\frac{66.666\ \text{MHz}}{\text{BulkSystemClockDivider}}$
BulkBaudRate	Selects a predefined baud rate or programmable option for the selected UART.

Table 21: GenICam Features Available for Serial Communication (Continued)

Feature	Description
BulkBaudRateFactor	Programs a user defined baud rate for the selected UART.
BulkBaudRateValue	Displays the programmed baud rate for the selected UART.
BulkLoopback	Receives serial data sent from a host PC application to the video interface and loops it back to the host PC application.
BulkNumOfStopBits	Selects a stop bit option (either 1 or 2).
BulkParity	Selects a parity option (None, Even, or Odd).
BulkUpstreamFifoWatermark	Sets the level of upstream FIFO at which a USB3 Vision event is generated. This feature controls the number of bytes that can be accumulated in the bulk interface upstream FIFO before the NTx-U3 delivers them to the host using an event type packet.

Chapter 7

Pixel Bus Definitions and Timing

This chapter describes the interface responsible for transmitting data from the camera to the NTx-U3.

The following topics are covered in this chapter:

Pixel Bus Definitions

The tables in this section list the NTx-U3 pixel bus definitions.

Mono/RGB/Bayer/Truesense Sparse Color Filter

Table 22: Mono/RGB/Bayer/Truesense Sparse Color Filter Pixel Bus Definitions

	Mono8 / Bayer8/ SCF1WGWR8		Mono10 / Bayer10/ SCF1WGWR10		Mono12 / Bayer12/ SCF1WGWR12		Mono14 / SCF1WGWR14		Mono16 / Bayer16		BGR8		RGB8	
	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Comp.	Bit	Comp.	Bit
PB_Data 0	0	0	0	0	0	0	0	0	0	0	B0	0	R0	0
PB_Data 1	0	1	0	1	0	1	0	1	0	1	B1	1	R1	1
PB_Data 2	0	2	0	2	0	2	0	2	0	2	B2	2	R2	2
PB_Data 3	0	3	0	3	0	3	0	3	0	3	B3	3	R3	3
PB_Data 4	0	4	0	4	0	4	0	4	0	4	B4	4	R4	4
PB_Data 5	0	5	0	5	0	5	0	5	0	5	B5	5	R5	5
PB_Data 6	0	6	0	6	0	6	0	6	0	6	B6	6	R6	6
PB_Data 7	0	7	0	7	0	7	0	7	0	7	B7	7	R7	7
PB_Data 8	1	0	0	8	0	8	0	8	0	8	G0	0	G0	0
PB_Data 9	1	1	0	9	0	9	0	9	0	9	G1	1	G1	1
PB_Data 10	1	2	-	nc	0	10	0	10	0	10	G2	2	G2	2
PB_Data 11	1	3	-	nc	0	11	0	11	0	11	G3	3	G3	3
PB_Data 12	1	4	1	8	1	8	0	12	0	12	G4	4	G4	4
PB_Data 13	1	5	1	9	1	9	0	13	0	13	G5	5	G5	5
PB_Data 14	1	6	-	nc	1	10	-	nc	0	14	G6	6	G6	6
PB_Data 15	1	7	-	nc	1	11	-	nc	0	15	G7	7	G7	7
PB_Data 16	2	0	1	0	1	0	-	nc	1	0	R0	0	B0	0
PB_Data 17	2	1	1	1	1	1	-	nc	1	1	R1	1	B1	1
PB_Data 18	2	2	1	2	1	2	-	nc	1	2	R2	2	B2	2
PB_Data 19	2	3	1	3	1	3	-	nc	1	3	R3	3	B3	3
PB_Data 20	2	4	1	4	1	4	-	nc	1	4	R4	4	B4	4
PB_Data 21	2	5	1	5	1	5	-	nc	1	5	R5	5	B5	5
PB_Data 22	2	6	1	6	1	6	-	nc	1	6	R6	6	B6	6
PB_Data 23	2	7	1	7	1	7	-	nc	1	7	R7	7	B7	7

Table 22: Mono/RGB/Bayer/Truesense Sparse Color Filter Pixel Bus Definitions (Continued)

	Mono8 / Bayer8/ SCF1WGWR8		Mono10 / Bayer10/ SCF1WGWR10		Mono12 / Bayer12/ SCF1WGWR12		Mono14 / SCF1WGWR14		Mono16 / Bayer16		BGR8		RGB8	
	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Tap	Bit	Comp.	Bit	Comp.	Bit
PB_Data 24	3	0	-	nc	-	nc	-	nc	1	8	-	nc	-	nc
PB_Data 25	3	1	-	nc	-	nc	-	nc	1	9	-	nc	-	nc
PB_Data 26	3	2	-	nc	-	nc	-	nc	1	10	-	nc	-	nc
PB_Data 27	3	3	-	nc	-	nc	-	nc	1	11	-	nc	-	nc
PB_Data 28	3	4	-	nc	-	nc	-	nc	1	12	-	nc	-	nc
PB_Data 29	3	5	-	nc	-	nc	-	nc	1	13	-	nc	-	nc
PB_Data 30	3	6	-	nc	-	nc	-	nc	1	14	-	nc	-	nc
PB_Data 31	3	7	-	nc	-	nc	-	nc	1	15	-	nc	-	nc

YUV411_8_UYYVYY: 1 Tap

Table 23: YUV411_8_UYYVYY: 1 Tap Pixel Bus Definitions

	Clock 1		Clock 2		Clock 3		Clock 4	
	Component	Bit	Component	Bit	Component	Bit	Component	Bit
PB_Data 0	Y11	0	Y11	4	Y13	0	Y13	4
PB_Data 1	Y11	1	Y11	5	Y13	1	Y13	5
PB_Data 2	Y11	2	Y11	6	Y13	2	Y13	6
PB_Data 3	Y11	3	Y11	7	Y13	3	Y13	7
PB_Data 4	U11	0	Y12	0	V11	0	Y14	0
PB_Data 5	U11	1	Y12	1	V11	1	Y14	1
PB_Data 6	U11	2	Y12	2	V11	2	Y14	2
PB_Data 7	U11	3	Y12	3	V11	3	Y14	3
PB_Data 8	U11	4	Y12	4	V11	4	Y14	4
PB_Data 9	U11	5	Y12	5	V11	5	Y14	5
PB_Data 10	U11	6	Y12	6	V11	6	Y14	6
PB_Data 11	U11	7	Y12	7	V11	7	Y14	7
PB_Data 12 through to PB_Data 31	-	-	-	-	-	-	-	-

YUV411_8_UYYVYY/YCbCr709_411_8_CbYYCrYY: 2 Tap

Table 24: YUV411_8_UYYVYY/YCbCr709_411_8_CbYYCrYY: 2 Tap Pixel Bus Definitions

	Clock 1		Clock 2		Clock 3		Clock 4	
	Component	Bit	Component	Bit	Component	Bit	Component	Bit
PB_Data 0	Y11	0	Y13	0	Y15	0	Y17	0
PB_Data 1	Y11	1	Y13	1	Y15	1	Y17	1
PB_Data 2	Y11	2	Y13	2	Y15	2	Y17	2
PB_Data 3	Y11	3	Y13	3	Y15	3	Y17	3
PB_Data 4	U11	0	V11	0	U15	0	V15	0
PB_Data 5	U11	1	V11	1	U15	1	V15	1
PB_Data 6	U11	2	V11	2	U15	2	V15	2
PB_Data 7	U11	3	V11	3	U15	3	V15	3
PB_Data 8	U11	4	V11	4	U15	4	V15	4
PB_Data 9	U11	5	V11	5	U15	5	V15	5
PB_Data 10	U11	6	V11	6	U15	6	V15	6
PB_Data 11	U11	7	V11	7	U15	7	V15	7
PB_Data 12	Y12	4	Y14	4	Y16	4	Y18	4
PB_Data 13	Y12	5	Y14	5	Y16	5	Y18	5
PB_Data 14	Y12	6	Y14	6	Y16	6	Y18	6
PB_Data 15	Y12	7	Y14	7	Y16	7	Y18	7
PB_Data 16	Y11	4	Y13	4	Y15	4	Y17	4
PB_Data 17	Y11	5	Y13	5	Y15	5	Y17	5
PB_Data 18	Y11	6	Y13	6	Y15	6	Y17	6
PB_Data 19	Y11	7	Y13	7	Y15	7	Y17	7
PB_Data 20	Y12	0	Y14	0	Y16	0	Y18	0
PB_Data 21	Y12	1	Y14	1	Y16	1	Y18	1
PB_Data 22	Y12	2	Y14	2	Y16	2	Y18	2
PB_Data 23	Y12	3	Y14	3	Y16	3	Y18	3
PB_Data 24 through to PB_Data 31	-	-	-	-	-	-	-	-

YUV422_8_UYVY/YCbCr422_8_CbYCrY/YCbCr709_422_8_CbYCrY

Depending on how you configure the **PixelBusTimeSlotsCount** feature, pixel data can be sent to one or two pixel clocks.

Table 25: YUV422_8_UYVY/YCbCr422_8_CbYCrY/YCbCr709_422_8_CbYCrY Pixel Bus Definitions (PixelBusTimeSlotsCount = One)

	Clock 1		Clock 2		Clock 3		Clock 4	
	Component	Bit	Component	Bit	Component	Bit	Component	Bit
PB_Data 0	U11	0	V11	0	U13	0	V13	0
PB_Data 1	U11	1	V11	1	U13	1	V13	1
PB_Data 2	U11	2	V11	2	U13	2	V13	2
PB_Data 3	U11	3	V11	3	U13	3	V13	3
PB_Data 4	U11	4	V11	4	U13	4	V13	4
PB_Data 5	U11	5	V11	5	U13	5	V13	5
PB_Data 6	U11	6	V11	6	U13	6	V13	6
PB_Data 7	U11	7	V11	7	U13	7	V13	7
PB_Data 8	Y11	0	Y12	0	Y13	0	Y14	0
PB_Data 9	Y11	1	Y12	1	Y13	1	Y14	1
PB_Data 10	Y11	2	Y12	2	Y13	2	Y14	2
PB_Data 11	Y11	3	Y12	3	Y13	3	Y14	3
PB_Data 12	Y11	4	Y12	4	Y13	4	Y14	4
PB_Data 13	Y11	5	Y12	5	Y13	5	Y14	5
PB_Data 14	Y11	6	Y12	6	Y13	6	Y14	6
PB_Data 15	Y11	7	Y12	7	Y13	7	Y14	7
PB_Data 16 through to PB_Data 31	-	-	-	-	-	-	-	-

See the next page for Table 26: "YUV422_8_UYVY/YCbCr422_8_CbYCrY/ YCbCr709_422_8_CbYCrY Pixel Bus Definitions (PixelBusTimeSlotsCount = Two)".

Table 26: YUV422_8_UYVY/YCbCr422_8_CbYCrY/YCbCr709_422_8_CbYCrY Pixel Bus Definitions (PixelBusTimeSlotsCount = Two)

	Clock 1		Clock 2		Clock 3		Clock 4		Clock 5		Clock 6	
	Comp.	Bit	Comp.	Bit	Comp.	Bit	Comp.	Bit	Comp.	Bit	Comp.	Bit
PB_Data 0	U11	0	Y11	0	V11	0	Y12	0	U13	0	Y13	0
PB_Data 1	U11	1	Y11	1	V11	1	Y12	1	U13	1	Y13	1
PB_Data 2	U11	2	Y11	2	V11	2	Y12	2	U13	2	Y13	2
PB_Data 3	U11	3	Y11	3	V11	3	Y12	3	U13	3	Y13	3
PB_Data 4	U11	4	Y11	4	V11	4	Y12	4	U13	4	Y13	4
PB_Data 5	U11	5	Y11	5	V11	5	Y12	5	U13	5	Y13	5
PB_Data 6	U11	6	Y11	6	V11	6	Y12	6	U13	6	Y13	6
PB_Data 7	U11	7	Y11	7	V11	7	Y12	7	U13	7	Y13	7
PB_Data 8-31	-	-	-	-	-	-	-	-	-	-	-	-

YUV8_UYV

Table 27: YUV8_UYV Pixel Bus Definitions

	Clock 1		Clock 3	
	Component	Bit	Component	Bit
PB_Data 0	U11	0	U12	0
PB_Data 1	U11	1	U12	1
PB_Data 2	U11	2	U12	2
PB_Data 3	U11	3	U12	3
PB_Data 4	U11	4	U12	4
PB_Data 5	U11	5	U12	5
PB_Data 6	U11	6	U12	6
PB_Data 7	U11	7	U12	7
PB_Data 8	Y11	0	Y12	0
PB_Data 9	Y11	1	Y12	1
PB_Data 10	Y11	2	Y12	2
PB_Data 11	Y11	3	Y12	3
PB_Data 12	Y11	4	Y12	4
PB_Data 13	Y11	5	Y12	5
PB_Data 14	Y11	6	Y12	6
PB_Data 15	Y11	7	Y12	7
PB_Data 16	V11	0	V12	0
PB_Data 17	V11	1	V12	1
PB_Data 18	V11	2	V12	2
PB_Data 19	V11	3	V12	3
PB_Data 20	V11	4	V12	4
PB_Data 21	V11	5	V12	5
PB_Data 22	V11	6	V12	6
PB_Data 23	V11	7	V12	7
PB_Data 24 through to PB_Data 31	-	-	-	-

Pixel Bus Timing

The pixel bus transmits data from the camera to the NTx-U3 in a format similar to deserialized Camera Link Standard data, as shown in the following image.

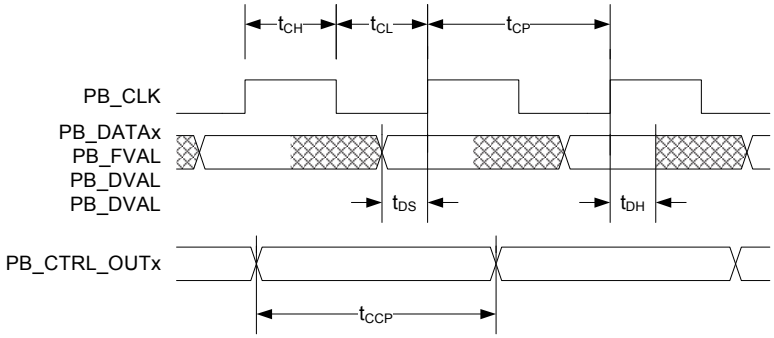


Table 28: Sub-Clock Delays on the Camera Interface

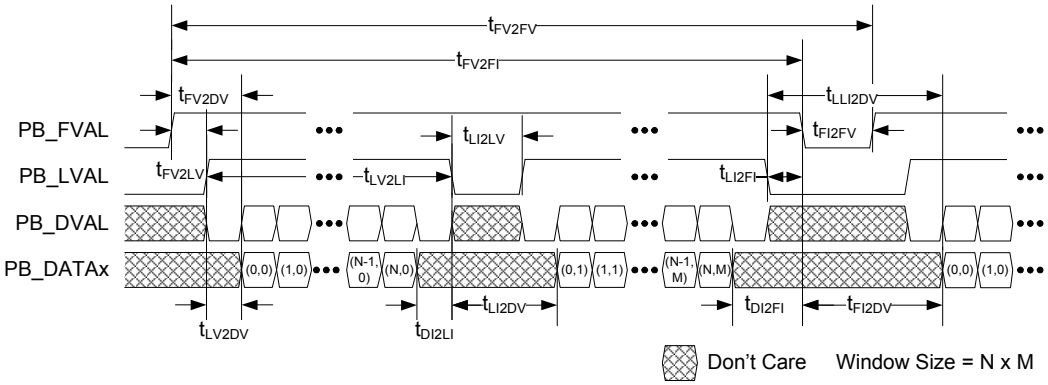
Parameter	Symbol	Minimum	Maximum	Notes
PB_CLK high-level width	t_{CH}	4.1 ns	N/A	N/A
PB_CLK low-level width	t_{CL}	4.1 ns	N/A	N/A
PB_CLK frequency	f_{CP}	20 MHz	120 MHz*	N/A
PB_CLK clock period	t_{CP}	8.3 ns	N/A	N/A
PB_DATAx setup time	t_{DS}	2 ns	N/A	By design
PB_DATAx hold time	t_{DH}	2 ns	N/A	By design
PB_CTRL_OUTx pulse width	t_{CCP}	30 ns	N/A	

*To ensure optimal performance, ensure that the output data rate does not exceed 3.2 Gbps.

Pixel Bus Signals

The output of the camera must match the format of the NTx-U3. You should select a case for your application and then refer to "Timing Values for All Cases" on page 58.

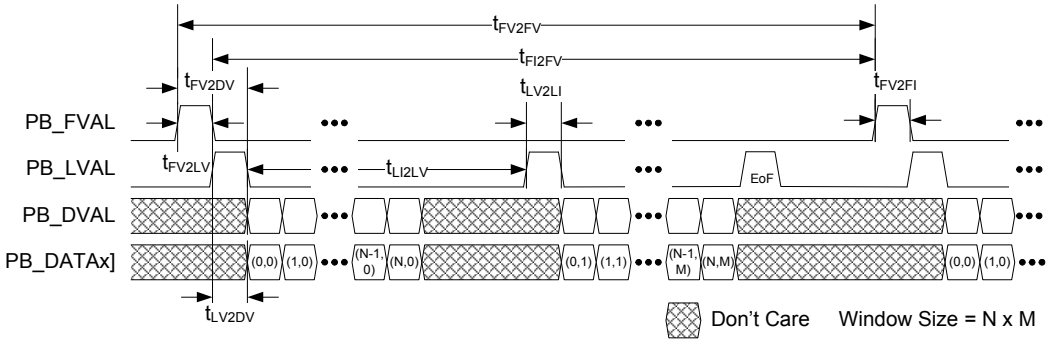
Case 1: FVAL and LVAL are Level-Sensitive



Case 2: FVAL and LVAL are Edge-Sensitive

In this case, FVAL and LVAL are edge-sensitive.

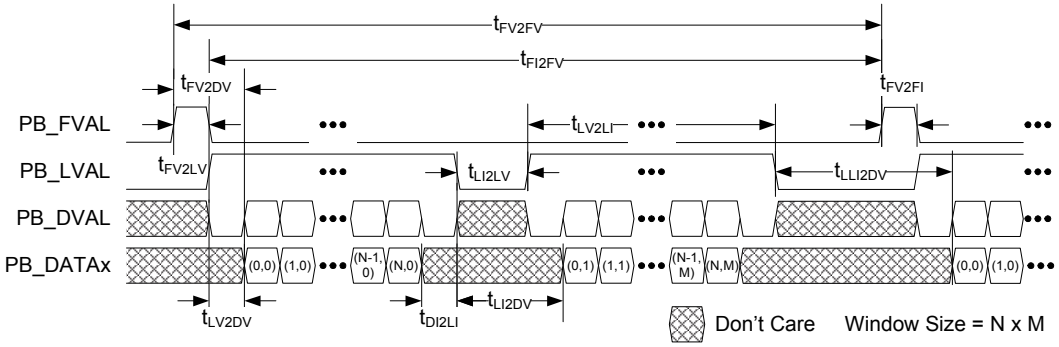
- **Start of frame/line is signaled by:** A rising (or falling) edge on FVAL, which signals the start of a *frame*. A rising (or falling) edge on LVAL, which signals the start of a *line*.
- **End of frame is signaled by:**
  - The next FVAL valid edge (rising edge when rising-edge sensitive or falling edge when falling-edge sensitive) occurs.
  - Or, when all of the pixels have been acquired (as set in the image height and width settings) **AND** an end-of-frame (EOF) occurs.
    Note: EOF occurs at LVAL rising edge (when rising-edge sensitive) or LVAL falling edge (when falling-edge sensitive). This is an additional LVAL edge, in addition to the configured/expected number of lines. See the EOF indicator in the illustration below.
- **Line Missing status and Partial Line Missing errors:** Partial Line Missing indicates lines are ending early (the next LVAL valid edge occurs before all of the pixels have been acquired). Full Line Missing indicates that the frame is ending early (the next FVAL edge occurs before all of the lines have been acquired).



Case 3: FVAL is Edge-Sensitive and LVAL is Level-Sensitive

In this case, FVAL is edge-sensitive and LVAL is level-sensitive.

- **Start of frame/line is signaled by:** A rising (or falling) edge on FVAL, which signals start of *frame*. The line is valid when LVAL is active (high or low depending on settings).
- **End of frame is signaled by:**
  - The next FVAL valid edge (rising edge when rising-edge sensitive or falling edge when falling-edge sensitive) occurs.
  - Or when all of the lines have been acquired (as set in the image height settings) **AND** the last LVAL with valid data is de-asserted (low when high level sensitive or high when low level sensitive).
- **Line Missing status or a Partial Line Missing error generated:**
  - Full Line Missing indicates that the frame is ending early (the next FVAL edge occurs before all of the lines have been acquired). Partial Line Missing indicates that lines are ending early (in this case, LVAL is de-asserted before all pixels in a line are captured).



Timing Values for All Cases

The TCP (PB0_CLK period) timing values listed in the following table are minimum values only.

Table 29: TCP Timing Values for All Cases

From	To	Symbol	Case 1 (level) (t_{cp})	Case 2 (edge) (t_{cp})	Case 3 (both) (t_{cp})
FVAL valid	LVAL valid [a]	t_{FV2LV}	0 [b]	0	1
FVAL valid	Data valid [a,c,d]	t_{FV2DV}	0 [b]	16 [f]	1
LVAL valid	Data valid [a,c,d]	t_{LV2DV}	0	1	0
LVAL valid	LVAL invalid [a]	t_{LV2LI}	1	1	1
LVAL invalid	LVAL valid [a]	t_{LI2LV}	1	1	1
Data invalid	LVAL invalid [a,c,d]	t_{DI2LI}	0	N/A	0
LVAL invalid	FVAL invalid [a]	t_{LI2FI}	0 [e]	N/A	N/A
Data invalid	FVAL invalid [a,c,d]	t_{DI2FI}	0 [e]	N/A	N/A
FVAL invalid	FVAL valid [a]	t_{FI2FV}	1	1	1
FVAL invalid	Data valid [a,c,d]	t_{FI2DV}	1	N/A	N/A
Last LVAL invalid	Data valid	t_{LLI2DV}	16 [f]	N/A	16 [f]
FVAL valid	FVAL invalid	t_{FV2FI}	16 [f]	1	1
FVAL valid	FVAL valid	t_{2FV2FV}	17 [f]	17 [f]	17 [f]

a. The valid state of FVAL and LVAL is high when they are set as level-high sensitive or rising-edge sensitive. Their valid state is low when they are set as level-low sensitive or falling-edge sensitive.

b. If LVAL is valid before FVAL becomes valid, the grabber drops the full line.

c. Data valid is defined by FVAL valid (note a), LVAL valid (note a), and DVAL valid (note d).

d. The valid state of DVAL is high when it is set as level-high sensitive, and low when set as level-low sensitive. DVAL is always valid in the grabber when the PixelBusDataValidEnabled feature is off.

e. If FVAL becomes invalid and LVAL is still valid, the line is truncated.

f. This is a worst-case value. Subtract 3 cycles if the pixel type is 8-bit, 1-tap. Subtract 1 cycle for all other pixel types except 10/12- bit, 2-tap, unpacked, and RGB unpacked. Subtract up to 7 cycles if the image size is a multiple of 32 bytes.

Chapter 8

Signal Handling

The NTx-U3 includes a programmable logic controller (PLC) that lets you control external machines and react to inputs. By controlling your system using the PLC, you can make functional changes, adjust timing, or add features without having to add new hardware.

PLC Programming Signals

For an introduction to the PLC and for detailed information about how PLC signals are handled, see the *iPORT Advanced Features User Guide*, available on the Pleora Support Center at www.pleora.com.

The following table lists the PLC input and output programming signals that are specific to the NTx-U3, and indicates the pins on which they are available.

Table 30: PLC Signal Usage

Signal name	PLC equation usage	Associated pin
Pb0Fval	Input	Pin 75 (PB0_FVAL) on the 100-pin user circuitry connector.
Pb0Lval	Input	Pin 90 (PB0_LVAL) on the 100-pin user circuitry connector.
Pb0Dval	Input	Pin 78 (PB0_DVAL) on the 100-pin user circuitry connector.
Pb0Spare	Input	Pin 87 (PB0_MVAL) on the 100-pin user circuitry connector.
GpioIn0	Input	Pin 10 (GPIO_CONN_IN0) on the 12-pin circular connector.
GpioIn1	Input	Pin 8 (GPIO_CONN_IN1) on the 12-pin circular connector.
GpioIn2	Input	Pin 6 (GPIO_CONN_IN2) on the 12-pin circular connector.
GpioIn3	Input	Pin 3 (GPIO_CONN_IN3) on the 12-pin circular connector.
BufferWM0	Input	No associated pin
Grb0AcqActive	Input	No associated pin
PlcCtrl0	Input	No associated pin
PlcCtrl1	Input	No associated pin
PlcCtrl2	Input	No associated pin
PlcCtrl3	Input	No associated pin
Pb0CC0	Input, output	Pin 63 (PB0_CTRL_OUT0) on the 100-pin user circuitry connector.
Pb0CC1	Input, output	Pin 66 (PB0_CTRL_OUT1) on the 100-pin user circuitry connector.
Pb0CC2	Input, output	Pin 95 (PB0_CTRL_OUT2) on the 100-pin user circuitry connector.
Pb0CC3	Input, output	Pin 97 (PB0_CTRL_OUT3) on the 100-pin user circuitry connector.
GpioOut0	Input, output	Pin 9 (GPIO_CONN_OUT0) on the 12-pin circular connector.
GpioOut1	Input, output	Pin 7 (GPIO_CONN_OUT1) on the 12-pin circular connector.
GpioOut2	Input, output	Pin 4 (GPIO_CONN_OUT2) on the 12-pin circular connector.
PlcFval0	Input, output	No associated pin

Table 30: PLC Signal Usage (Continued)

Signal name	PLC equation usage	Associated pin
PlcLval0	Input, output	No associated pin
PlcMval0	Input, output	No associated pin
PlcTrig0	Input, output	No associated pin
PlcTimestampCtrl	Input, output	No associated pin
Timer0Trig	Input, output	No associated pin
Timer0Out	Input	No associated pin
Timer1Trig	Input, output	No associated pin
Timer1Out	Input	No associated pin
Counter0Reset	Input, output	No associated pin
Counter0Inc	Input, output	No associated pin
Counter0Dec	Input, output	No associated pin
Counter0Eq	Input	No associated pin
Counter0Gt	Input	No associated pin
Counter1Reset	Input, output	No associated pin
Counter1Inc	Input, output	No associated pin
Counter1Dec	Input, output	No associated pin
Counter1Eq	Input	No associated pin
Counter1Gt	Input	No associated pin
Rescaler0In	Input, output	No associated pin
Rescaler0Out	Input	No associated pin
Delayer0In	Input, output	No associated pin
Delayer0Out	Input	No associated pin
Event0	Input, output	No associated pin
Event1	Input, output	No associated pin
Event2	Input, output	No associated pin
Event3	Input, output	No associated pin

Chapter 9

Installing the eBUS SDK

This chapter describes how to install the eBUS SDK, and also provides information about installing the required driver.

Before you can configure and control your NTx-U3, you must install the eBUS SDK and USB3 Vision driver.

The following topics are covered in this chapter:

Installing the eBUS SDK

You can install the Pleora Technologies eBUS SDK on your computer to configure and control your NTx-U3.

The eBUS SDK includes:

- Pleora's eBUS Player application, which allows you to control the NTx-U3 parameters and view video from a video source connected to the NTx-U3.
- An extensive library of sample applications, with source code, to create working applications for device configuration and control, image and data acquisition, and image display and diagnostics.
- Drivers that optimize the performance of your system.

It is possible for you to configure the NTx-U3 and USB3 Vision compliant video sources using other GenICam compliant software, however, this guide provides you with the instructions you need to use the Pleora eBUS Player application.

Installing the eBUS Universal Pro Driver

The eBUS SDK includes a USB3 Vision driver that allows for configuration and control of USB3 Vision devices. The driver must be installed before you can use eBUS Player or any third-party SDK software to configure the NTx-U3. If it is not installed, the software will not detect the NTx-U3.

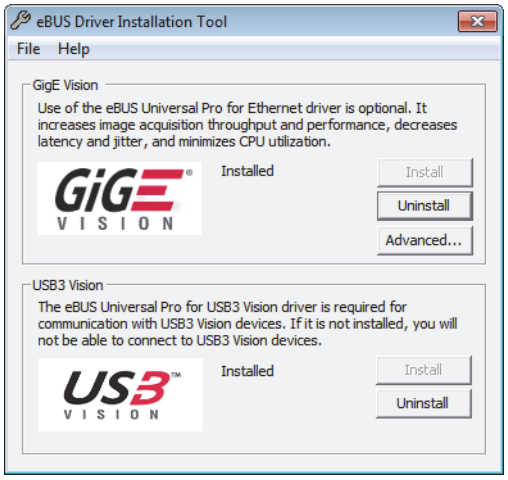
The GigE Vision driver, which is available during the installation of the eBUS SDK, is for use with GigE Vision devices, such as the Pleora NTx-GigE External Frame Grabber. The driver enhances existing general-purpose drivers shipped with NICs, increases image acquisition throughput and performance, decreases latency and jitter, and minimizes CPU utilization.

The drivers are selected for installation by default during the eBUS SDK installation process. If you choose not to install the drivers (or want to uninstall either driver), you can use the eBUS Driver Installation Tool.

To use the eBUS Driver Installation Tool

1. Click **Start** > **All Programs** > **eBUS** > **eBUS Driver Installation Tool**.
2. Under **USB3 Vision**, click **Install** or **Uninstall**.

   After a moment, the driver status changes. The driver is installed across all USB3 Vision devices on your computer.



3. Close the eBUS Driver Installation Tool.

   You may be required to restart your computer.

To see the versions of the installed drivers, click **Help** > **About**.

Chapter 10

Connecting to the NTx-U3 and Configuring General Settings

After you have set up the physical connections to the NTx-U3, you can start eBUS Player to configure image settings to ensure images are received and displayed properly. You can also configure the buffer options to reduce the likelihood of lost packets.

eBUS Player is documented in more detail in the *eBUS Player User Guide*. The *iPORT NTx-U3 Embedded Video Interface User Guide* provides you with the eBUS Player instructions and overviews required to set up and configure the NTx-U3.

The following topics are covered in this chapter:

Confirming Image Streaming

The NTx-U3 can communicate with your computer using either a direct connection or by connecting to a USB 3.0 port on your computer.

To connect the cables and apply power

- Connect the NTx-U3 to a USB 3.0 port on your computer using a USB 3.0 A to Micro-B Y-cable.

To start eBUS Player and connect to a device

1. Start eBUS Player from the Windows **Start** menu.
2. Click **Select/Connect**.
3. In the **Device Selection** dialog box, click the NTx-U3.
4. Click **OK**.

   eBUS Player is now connected to the NTx-U3.

To confirm image streaming

1. Click **Play** to stream live images or the test pattern.

   For information about using the test pattern, see "To turn the test pattern on or off" on page 70.
2. After you confirm that images are streaming, click **Stop**.

If images do not stream, see the tips provided in "System Troubleshooting" on page 85.

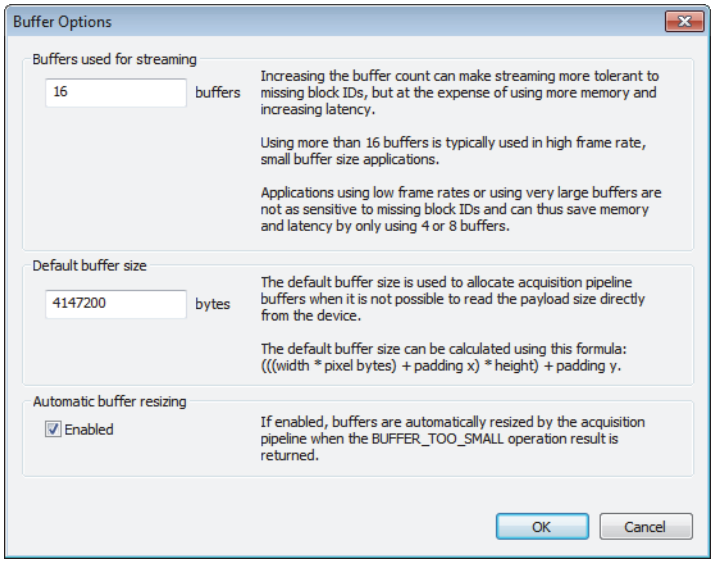
Configuring the Buffers

You can increase the buffer count using eBUS Player to make streaming more robust. A high number of buffers are needed in high frame rate applications, while a small number of buffers are needed for lower frame rates. Latency increases as the number of buffers increases.

To configure the buffers

1. Start eBUS Player and connect to the NTx-U3.
   For more information, see "To start eBUS Player and connect to a device" on page 68.
2. Click **Tools** > **Buffer Options**.
3. Click the buffer option that suits your requirements.
4. Click **OK**.

Default size for streaming is 16 buffers.



Configuring the Image Settings

You can configure the NTx-U3's image settings, which provide it with information about the image coming from the camera. These settings allow the images to appear correctly.

The image settings are located under **ImageFormatControl** in the **Device Control** dialog box.

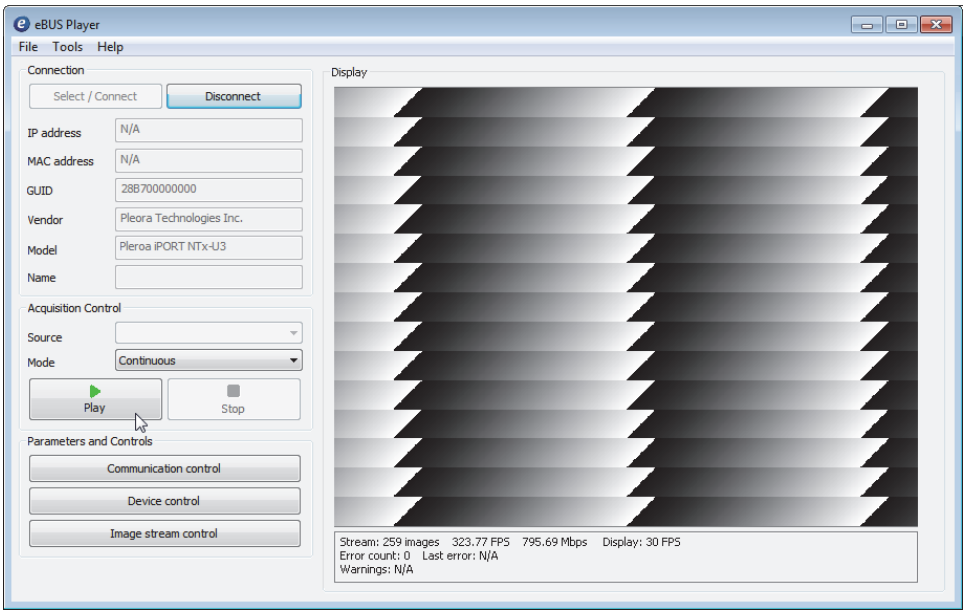
Changes that you make to the NTx-U3 are not persisted across power cycles, unless you use the **UserSetSave** feature. For information about saving settings to the NTx-U3's flash memory, see the *eBUS Player User Guide*, available on the Pleora Support Center.

To turn the test pattern on or off

1. Start eBUS Player and connect to the NTx-U3.

   For more information, see "To start eBUS Player and connect to a device" on page 68.
2. Under **Parameters and Controls**, click **Device control**.
3. Under **ImageFormatControl**, click a test pattern option in the list.
4. Close the **Device Control** dialog box.

   When the test pattern is enabled and you click **Play**, you will see an image similar to this (the pattern and colors may vary, depending on the image settings).

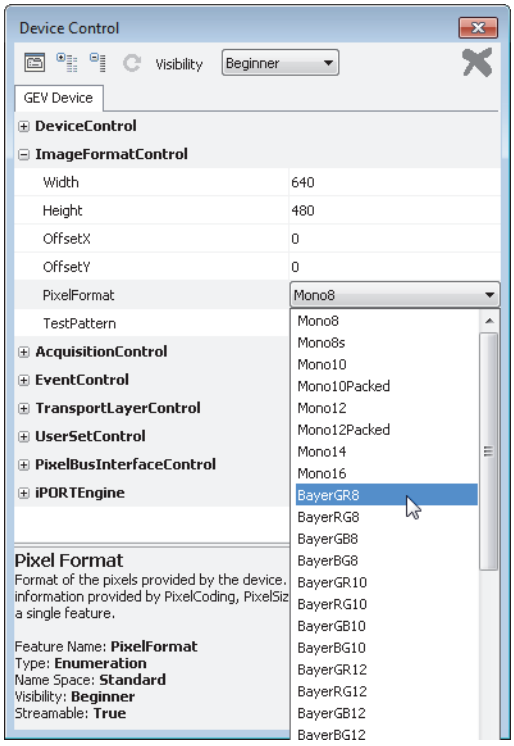


To change the pixel format

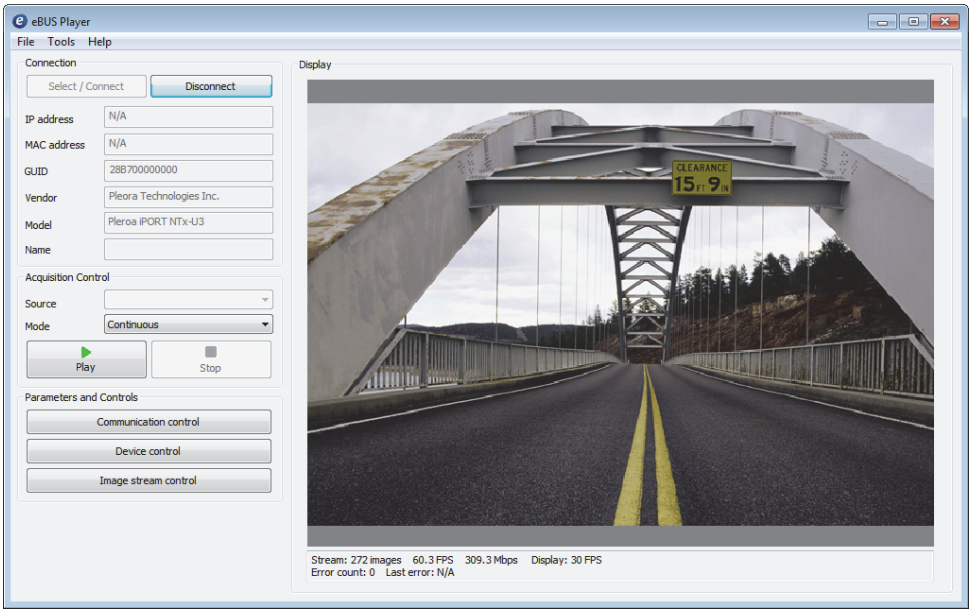
1. Start eBUS Player and connect to the NTx-U3.

   For more information, see "To start eBUS Player and connect to a device" on page 68.
2. If images are streaming, click the **Stop** button.
3. Under **Parameters and Controls**, click **Device control**.

4. Under **ImageFormatControl**, set the **PixelFormat** feature to a color format.



5. Close the **Device Control** dialog box.
6. Click **Play** to see the changes.



Example image. When the test pattern is enabled for the NTx-U3, a stream of moving lines will appear (often black, gray, and white) instead of video from your camera.

To configure the image width and height

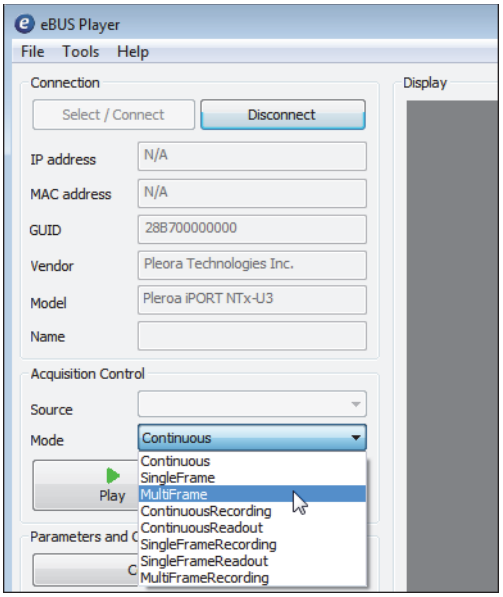
1. Start eBUS Player and connect to the NTx-U3.

   For more information, see "To start eBUS Player and connect to a device" on page 68.
2. If images are streaming, click the **Stop** button.
3. Under **Parameters and Controls**, click **Device control**.
4. Under **ImageFormatControl**, change the **Width** and **Height** to suit your camera.
5. Close the **Device Control** dialog box.

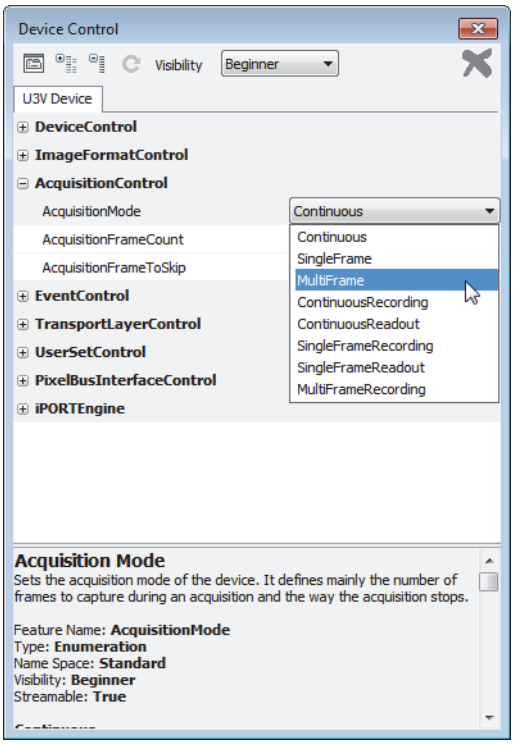
Configuring How Images are Acquired

Modes Standard on Most USB3 Vision-Compliant Devices

Continuous, SingleFrame, and MultiFrame modes are usually standard for embedded video interfaces. Acquisition starts when the **Play** button is pressed (the **AcquisitionStart** command is executed).



eBUS Player Main Page



Device Control Dialog Box

Recording and Readout Modes, Available on Pleora Devices

The **recording** acquisition modes allow you to capture images from a camera and store them in the NTx-U3's onboard memory. The **readout** acquisition modes allow images to be acquired from the device's memory at a slower rate, ensuring images are not lost.

These modes are helpful when you are working with a camera that transmits images at a rate that exceeds the connection between the NTx-U3 and the computer, resulting in dropped images. By using the recording and readout modes, you can capture and stream images from the camera without losing any images (as long as there is space in the onboard memory).

The recording acquisition modes (**ContinuousRecording**, **MultiFrameRecording**, and **SingleFrameRecording**) support back-to-back recording, which allows you to click the **Stop** and **Play** buttons multiple consecutive times without clearing the onboard memory.

Acquisition starts when the **Play** button is pressed (the **AcquisitionStart** command is executed) when one of the recording modes is selected.

Images can be stored in the NTx-U3's onboard memory as long as there is space or until there are 512 images in memory. For information about calculating how many images you can store, see "Calculating How Many Images Can be Stored in Onboard Memory" on page 77.

If the USB cable is disconnected, or if the computer is restarted, all captured images will be lost.

Understanding When Images are Removed from Onboard Memory

The following actions remove the images from the NTx-U3's onboard memory:

- Streaming images from the onboard memory using one of the readout acquisition modes (**ContinuousReadout** or **SingleFrameReadout**).
- Power cycling the device, which clears all images from the onboard memory.
- Making any of the following **AcquisitionMode** changes and then clicking the **Play** button (**AcquisitionStart** command):

Table 31: Changes that Clear Images from the Onboard Memory

First you acquire images with...	And then you change the Acquisition mode to...
ContinuousRecording, MultiFrameRecording, or SingleFrameRecording	Continuous, MultiFrame, or SingleFrame
SingleFrameReadout or ContinuousReadout	SingleFrame, MultiFrame, or Continuous
SingleFrameReadout or ContinuousReadout	ContinuousRecording, MultiFrameRecording, or SingleFrameRecording

ContinuousRecording Mode

With this mode, images are acquired continuously and are stored in the device's onboard memory until the memory is full (or 512 images are stored in onboard memory). When this limit is reached, the NTx-U3 stops acquiring new images from the camera.

We recommend that you observe **AcquisitionControl** > **BlockBufferCount** (**Expert** or **Guru** visibility level is required). When the value for this feature stops increasing, the memory is full. For information about the actions that clear the images from onboard memory, see "Understanding When Images are Removed from Onboard Memory" on page 74.

To determine how many images can be stored in memory, see "Calculating How Many Images Can be Stored in Onboard Memory" on page 77.

ContinuousReadout Mode

With this mode, images are continuously read (and removed) from the device's onboard memory. The readout begins at the first image in memory. To see the number of images stored in onboard memory, see **AcquisitionControl** > **BlockBufferCount** in the **Device Control** dialog box (**Expert** or **Guru** visibility level is required).

Readout continues until the **Stop** button is pressed (**AcquisitionStop** command is executed) or until the last image has been sent by the device (**BlockBufferCount** will be **0**).

MultiFrameRecording Mode

With this mode, a fixed number of images are stored in the device's onboard memory. To configure the number of images, set the **AcquisitionControl** > **AcquisitionFrameCount** feature in the **Device Control** dialog box. Images can be read out from memory using **ContinuousReadout** mode.

A maximum of 512 images can be acquired at one time in MultiFrameRecording mode.

To determine how many images can be stored in memory, see "Understanding When Images are Removed from Onboard Memory" on page 74.

If **AcquisitionControl** > **AcquisitionFrameCount** is set to a value that exceeds the amount of available memory, the NTx-U3 stops acquiring new images when the onboard memory is full (or 512 images are stored in onboard memory).

BlockBufferCount shows the number of images currently in memory. In MultiFrameRecording mode, this number is cumulative: If the memory is empty and you acquire an image, **BlockBufferCount** will match the **AcquisitionFrameCount**. If you stop and restart recording, **BlockBufferCount** will increment (to a maximum of 512 images, depending on the image size) and will no longer match the **AcquisitionFrameCount**.

For information about the actions that clear the images from onboard memory, see "Understanding When Images are Removed from Onboard Memory" on page 74.

SingleFrameRecording Mode

With this mode, a single image is saved in the NTx-U3's onboard memory after each **AcquisitionStart** command.

For information about the actions that clear the images from onboard memory, see "Understanding When Images are Removed from Onboard Memory" on page 74.

SingleFrameReadout Mode

With this mode, a single image is acquired from the NTx-U3's onboard memory.

Calculating How Many Images Can be Stored in Onboard Memory

First, take note of the **PayloadSize**, which appears under **TransportLayerControl** in the **Device Control** dialog box. Expert or Guru visibility level is required to access this feature.

The **PayloadSize** is automatically calculated by the device based on the selected image settings, which include Width, Height, OffsetX, OffsetY, PixelSize, any chunk data, as well as any padding that has to be added to the image payload.

For example, for a device configured to use Mono10p with images that are 1920 x 1080, the **PayloadSize** is equal to 2 592 000 bytes per image or 2.472 MB (2 592 000 / 1 048 576).

After determining **PayloadSize**, you can use the following equation to determine the number of images that can be saved in onboard memory:

Available onboard memory MB / PayloadSize MB = Number of images that can be saved

Using our example, the equation is:

120 MB / 2.472 MB = 48 images

Implementing the eBUS SDK

You can create your own image acquisition software for the NTx-U3. Consult the following guides for information about creating custom image acquisition software:

- *eBUS SDK API Quick Start Guides*, available for C++, .NET, Linux, and macOS, which are available on the Pleora Support Center at supportcenter.pleora.com.
- *eBUS SDK API Help Files*, which are installed on your computer during the installation of the eBUS SDK. You can access this documentation from the Windows Start menu under **eBUS SDK**.

Chapter 11

Reference: Mechanical Drawings and Material List

This chapter provides the mechanical drawings, and also provides a list of connectors and cables, with corresponding manufacturer details.

Three-dimensional (3-D) mechanical drawings are available at the Pleora Technologies Support Center.

The following topics are covered in this chapter:

Mechanical Drawings

The mechanical drawings in this section provide the NTx-U3's dimensions, features, and attributes. All dimensions are in millimeters. For the FPGA board and NTx-Mini prober board mechanical drawings, see "FPGA Board and NTx-Mini Prober Board Mechanical Drawings" on page 81.

Figure 3: USB PHY Board

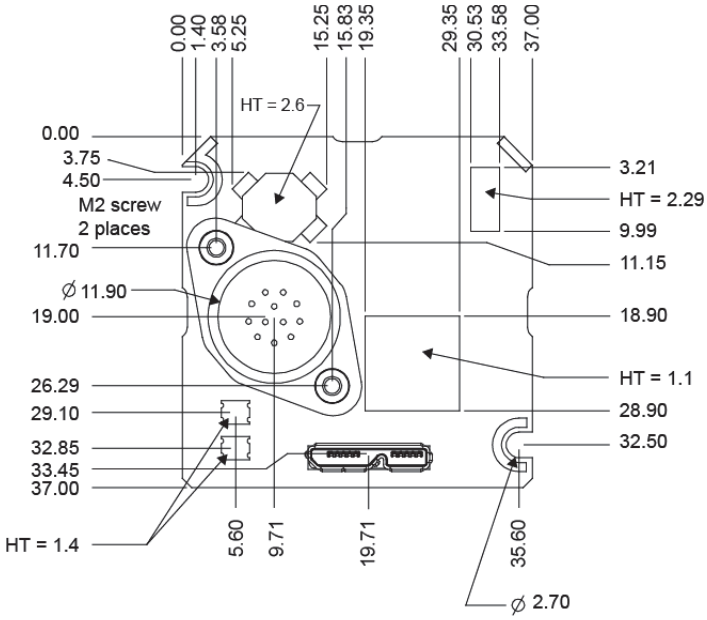


Figure 4: Board Set — Side Views

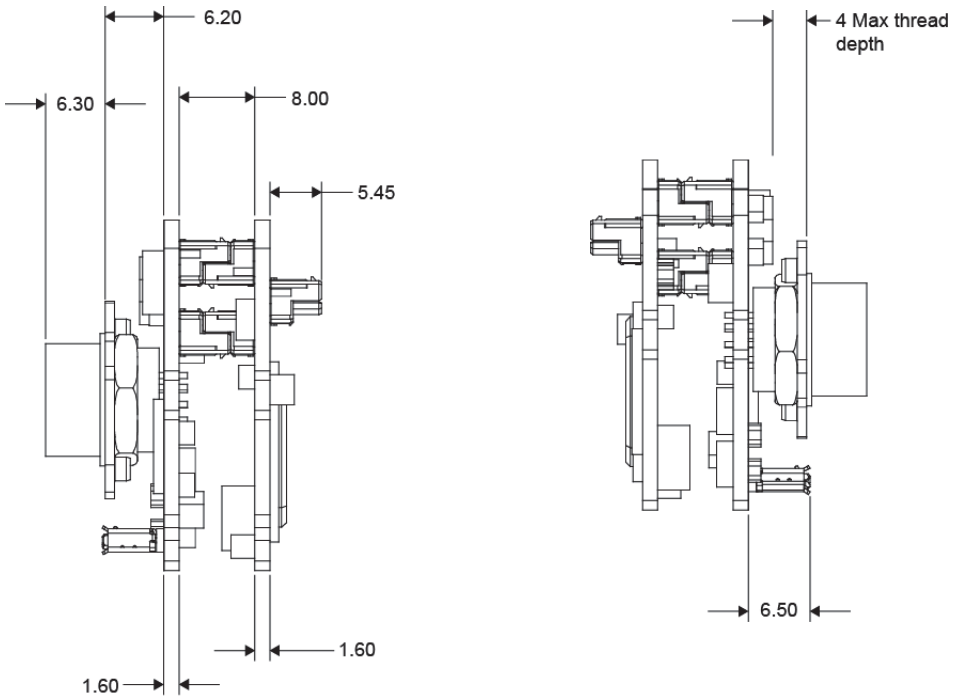
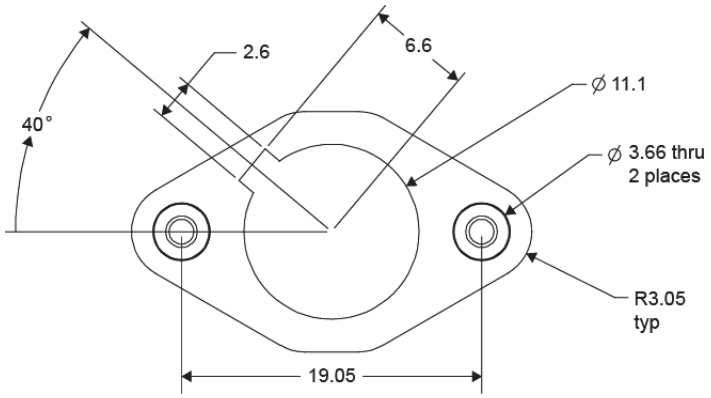


Figure 5: USB 3.0 Connector Flange



FPGA Board and NTx-Mini Prober Board Mechanical Drawings

The mechanical drawings in this section provide the dimensions, features, and attributes of the FPGA board and the NTx-Mini Prober board. All dimensions are in millimeters.

Figure 6: FPGA Board

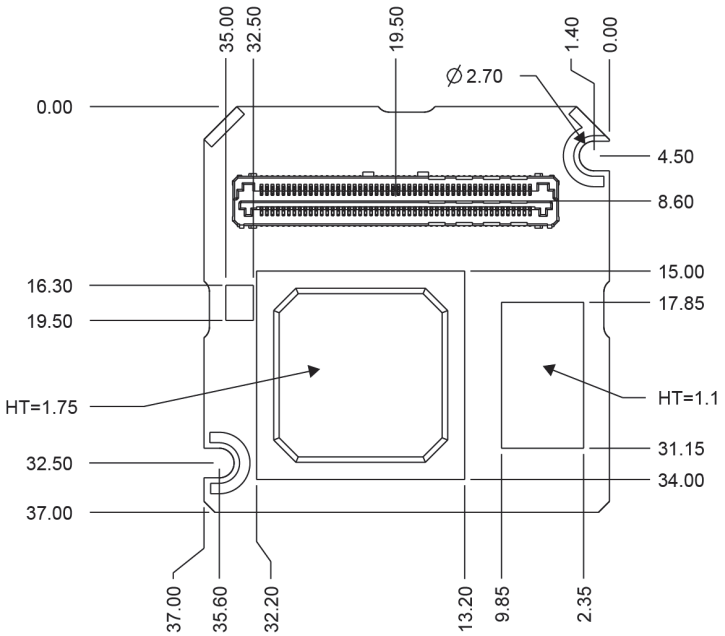
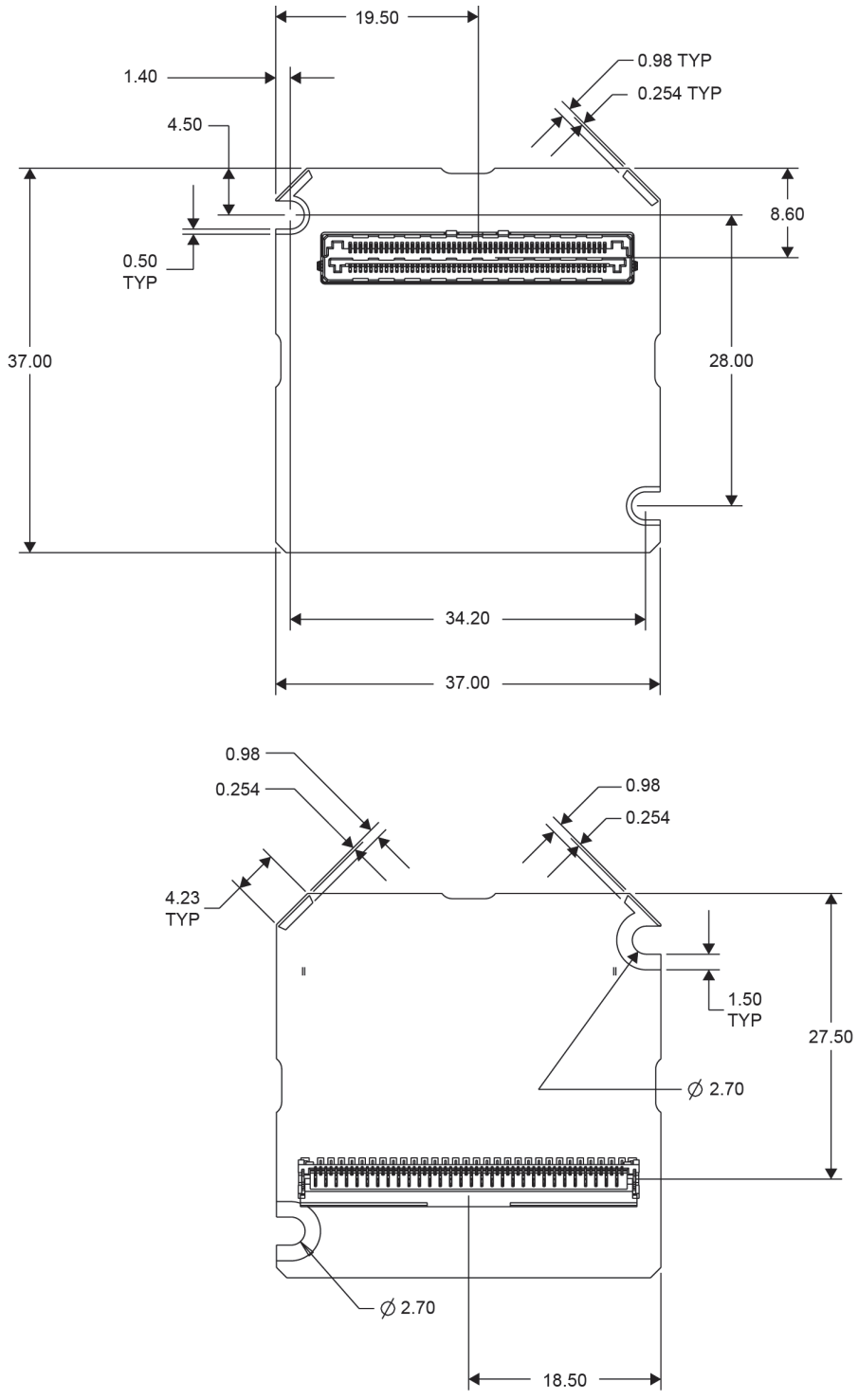


Figure 7: NTx-Mini Prober Board



Material List

The connector summaries for the NTx-U3 s are listed in the following table.

Table 32: Connector Summary

ID	Location	Description	Manufacturer part number	Manufacturer
J1	FPGA board	100-pin user circuitry interface. Samtec LSHM series 0.5mm pitch vertical 100-pin.	LSHM-150-04.0-L-DV-A-N-TR	Samtec
J5	USB PHY board	12-pin external interface	HR10A-10R-12PB(71)	Hirose
J1	USB PHY board	Micro-B USB 3.0 connector	897-10-010-00-300002	Mill-Max Mfg. Corp.
J2	GPIO board	20-pin FFC connector	FH33-20S-0.5SH(10)	Hirose
J3	USB PHY board	60-pin high speed hermaphroditic terminal/ socket strip	LSHM-130-04.0-L-DV-A-N-TR	Samtec
J3	FPGA board	60-pin connector	LSHM-130-04.0-L-DV-A-N-TR	Samtec

Source manufacturer, description, and identification may vary and are subject to change for each connector.

Chapter 12

System Troubleshooting

This chapter provides you with troubleshooting tips and recommended solutions for issues that can occur during configuration, setup, and operation of the NTx-U3. It also shows you how to switch between the backup and main firmware loads.

Not all scenarios and solutions are listed here. You can refer to the Pleora Technologies Support Center at www.pleora.com for additional support and assistance. Details for creating a customer account are available on the Pleora Technologies Support Center.

Refer to the product release notes that are available on the Pleora Technologies Support Center for known issues and other product features.

Troubleshooting Tips

The scenarios and known issues listed in this chapter are those that you might encounter during the setup and operation of your NTx-U3. Not all possible scenarios and errors are presented. The symptoms, possible causes, and resolutions depend upon your particular network, setup, and operation.

If you perform the resolution for your issue and the issue is not corrected, we recommend you review the other resolutions listed in this table. Some symptoms may be interrelated.

Table 33: Troubleshooting Tips

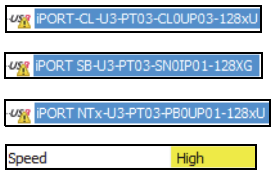
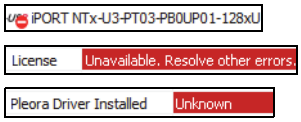
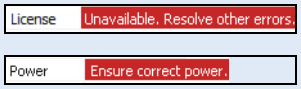
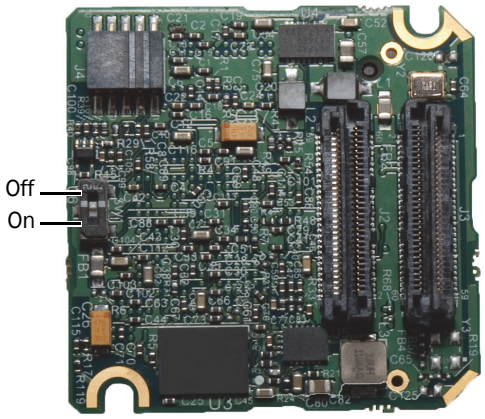
Symptom	Possible cause	Resolution
When selecting the NTx-U3 for connection, the **Speed** (in the **Device Selection** dialog box in eBUS Player) says **High** instead of **Super**, and a warning icon appears 	The NTx-U3 is connected to a USB 2.0 port on your computer, not a USB 3.0 port.	Connect the NTx-U3 to a USB 3.0 port on your computer.
	The USB 3.0 port may have experienced a power surge.	Troubleshoot the USB 3.0 port in your computer by: • Connecting the NTx-U3 to another USB 3.0 port on your computer. • Disconnecting the NTx-U3 from the computer and rebooting the computer.
When you connect the NTx-U3 to a USB port on your computer, a Windows warning appears, indicating that the driver could not be installed	The Pleora USB3 Vision driver is not installed on your computer.	Install the Pleora USB3 Vision driver on your computer using the eBUS Driver Installation Tool (**Start** > **All Programs** > **Pleora Technologies Inc** > **eBUS SDK** > **eBUS Driver Installation Tool**).
When selecting the NTx-U3 for connection, the **License** field (in the **Device Selection** dialog box in eBUS Player) says **Unavailable. Resolve other errors.** And the **Pleora Driver Installed** field says **Unknown** 	The Pleora USB3 Vision driver is not installed on your computer.	Install the Pleora USB3 Vision driver on your computer using the eBUS Driver Installation Tool.
The **License** field (in the **Device Selection** dialog box in eBUS Player) says **Invalid**.  The NTx-U3 appears in the **Device Selection** dialog box in eBUS Player but you cannot connect to it.	The Pleora USB3 Vision driver is not installed on your computer	Install the Pleora USB3 Vision driver on your computer using the eBUS Driver Installation Tool.
	If you have a third-party USB3 Vision driver on your computer, that driver may be interfering with the Pleora USB3 Vision driver's ability to recognize the NTx-U3.	Uninstall the third-party driver and install the Pleora USB3 Vision driver on your computer using the eBUS Driver Installation Tool.
	The USB host controller is shared, resulting in an inadequate power supply	Disconnect devices from your USB hub that are drawing power from the USB hub.
The **License** field (in the **Device Selection** dialog box in eBUS Player) says **Unlicensed. Watermark, limited use**.  A Pleora watermark appears on transmitted and received images.	Your camera does not use Pleora's technology for device control and to transmit and receive images.	Purchase a Pleora eBUS SDK license to license the camera and remove the watermark. For more information, visit www.pleora.com/products/ebus-sdk.

Table 33: Troubleshooting Tips (Continued)

Symptom	Possible cause	Resolution
Image errors appear as soon as you click **Play** and images do not stream	The NTx-U3 settings may not match the configuration of the image data that is being received from the camera.	Ensure the following NTx-U3 settings match the configuration of the image data from the camera: • DeviceScanType • SensorDigitizationTaps • PixelFormat • Width • Height
Images do not appear and the image count (located beside **Stream** at the bottom of eBUS Player) does not increase when you click **Play.**	The test pattern is off or no video source is available.	Turn the test pattern on. Or, connect a video source and ensure that **PixelBusInterfaceControl** > **PixelBusClockPresent** is **True**.
Dropped images, dropped connection, or failure to connect to the NTx-U3.	The power supply from the USB port may be inadequate.	Ensure 900 mA is available from the USB port. For more information, see "Powering the NTx-U3" on page 25.

Changing to the Backup Firmware Load

In some cases, you may need to change from the main firmware load to the backup firmware load. You can use the slide switch (SW1 on the FPGA board) to change to the backup firmware mode.



FPGA Board (Back View)

Table 34: Slide Switch Settings

Position	FPGA load
Off	Main load
On	Backup load

Chapter 13

Reference: Mean Time Between Failures (MTBF) Data

The following table provides MTBF data.

Table 35: MTBF Data

Model	MTBF @ 40°C
NTx-U3	1,277,505 hours

Assumptions:

1. The calculation is performed using the *RelCalc for Windows V5.1-TELC3* software, which implements Telcordia SR-332 (Issue 3) failure rate models.
2. The operating internal chassis temperature is 40°C. The calculation assumes the temperature across the boards is relatively constant.
3. The Telcordia environment is GB.
4. Each part's operating current/voltage/power stress is 50%.
5. The typical operating power value (as specified in the component's datasheet) is used for each IC and semiconductor.
6. The calculation uses the 90% UCL (Upper Confidence Level) Telcordia Issue 3 model.
7. Each part's Telcordia Quality Level is I.

Chapter 14

Technical Support

On the Pleora Support Center, you can:

- Download the latest software and firmware.
- Log a support issue.
- View documentation for current and past releases.
- Browse for solutions to problems other customers have encountered.
- Read knowledge base articles for information about common tasks.

To visit the Pleora Support Center

- Go to supportcenter.pleora.com and click **Support Center**.
  If you have not registered yet, you are prompted to register.
  Accounts are usually validated within one business day.