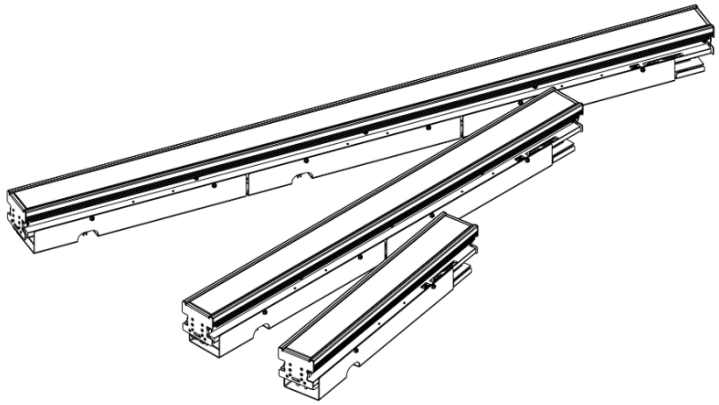
MITSUBISHI ELECTRIC

Changes for the Better

CONTACT IMAGE SENSOR (CIS)
KD Series for Web Surface Inspection

KD6R309AX4, KD6R617AX4, KD6R926AX4, KD6R335AX4

KD6R309AX4-NL, KD6R617AX4-NL, KD6R926AX4-NL



User's Manual

TM-XL550F

September 4, 2024

Design and specification are subject to change without notice.

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Camera Link is a trademark or registered trademark of AIA (Automated Imaging Association).

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Chapter 1 : Notice

1-1 RESTRICTION FOR USE

Thank you very much for purchasing Mitsubishi Electric Contact Image Sensor (CIS). This document contains information that introduces how to use this product appropriately and safely. Read through this document carefully before starting to use this product in your equipment or system.

This product is designed for the purpose of being used in general industries. Do not use this product for specific and particular applications (aerospace application, combustive equipment, transportation equipment, life-support system, safety device, etc.) where special quality and reliability are required and failure or malfunction could directly threaten people's lives, or do harm to the human body. Do not use for applications other than the purpose of being used in general industries intended by Mitsubishi Electric. If you plan to use for such particular applications, contact our sales department personnel before doing so. If you should use it for applications other than the general industries intended by Mitsubishi Electric without consulting our sales department personnel, Mitsubishi Electric SHALL HAVE NO RESPONSIBILITY OR LIABILITY (INCLUDING, BUT NOT LIMITEDTO ANY AND ALL RESPONSIBILITY OR LIABILITY BASED ON CONTRACT, WARRANTY, TORT, PRODUCT LIABILITY) FOR ANY INJURY OR DEATH TO PERSONS OR LOSS OR DAMAGE TOPROPERTY CAUSED BY the PRODUCT.

Determine the applicability of this product to your equipment or devices through an appropriate analysis or evaluation by the designer of such equipment or devices, or personnel related to the specification. Such designers or personnel shall warrant the performance and safety of your equipment or devices such as dust-proof, water-proof, EMC and EMI, by themselves.

Design, specification and the contents of this document are subject to change without notice.

1-2 PRECAUTIONS

For Safety Use.
Be aware of the following warnings and cautions to use this product appropriately and safely.

■Danger ,Warning and Caution

Danger	Ignoring this indication and handling it incorrectly poses an imminent risk of death or serious injury to the user.
Warning	Ignoring this indication and handling it incorrectly poses a possibility of death or serious injury to the user.
Caution	Ignoring this indication and handling it incorrectly poses a possibility of bodily injury or property damage.

■Indications and definitions

	This indicates the Danger, Warning or Caution described above.
	This indicates the prohibited action that must not be handled.
	This indicates the mandatory action that must be carried out.

	This indicates a prohibited action such as an operation in a place where this product may get wet.
	This indicates the prohibition of the disassembly of this product.
	This indicates the possibility of the injury under the specific situation

1-2 PRECAUTIONS

	Danger
	Do not operate this product in a place where it is explosive, combustible or inflammable. Operating in a place having propane gas, gasoline or flammable gas may cause a fire and/or an explosion.
	Use power supply having protection against overload. A fuse is mounted on the 5V power supply line of this product. If current higher than rated current flows during use, the fuse cut off the power supply to protect the product. However, depending on the power supply selection, if the product is overloaded and malfunctions, an excessive current may flow through the power supply and the product even momentarily. For product safety, we recommend using a power supply that is protected against overload.
	Stop operation when you find any abnormalities or defects. Otherwise, a fire or an electric shock may occur.
	Do not repair, disassemble and/or modify by yourself. Otherwise, a fire, defect, or an electric shock may occur. If you need to repair this product, you must contact the agency who sold you this product.
	Do not get this product wet. Handle this product with water-proofing. Otherwise, a defect or an electric shock may occur. This product is designated for indoor use. This product is designed as a line-scan module embedded in a system.
	Do not operate this product outdoors. This product is designed as a line-scan module embedded in a system. This product is designated for indoor use.

1-2 PRECAUTIONS

	Danger
	**Do not put anything on this product.** Otherwise, a fire or electrical shock may occur because of the things or materials (especially metals) in this product.
	**Do not put this product on an unstable surface, slanting and/or vibrating.** Otherwise, drop and/or fail of this product may cause injury.
	**Do not look at the internal illumination directly.** (Non-illumination models are not included.) This product comprises a bright illumination. There are some risks of eye damage.
	**Avoid the damage that ESD can cause. Never expose the internal electronics to a potentially hazardous environment. Do not handle this product with an insulation sheet or on wooden desk. In addition, do not cover this product with any materials having an electrostatic discharge.** Doing so may cause serious damage.
	**Be careful not to use this product vertically. ("vertically" means the long side is perpendicular to the floor.)** If it is used vertically, it may cause deterioration of performance or malfunction.

1-2 PRECAUTIONS

	Warning
	Do not store this product in the following places. ●In a vibrating or precarious place ●In a humid, smoky, vaporized or dusty place ●In a slanting place ●In a place exposed by direct sun light ●In a temperature varying place ●Near anything generating heat (eg. A stove, heater, etc) ●In a corrosive gas atmosphere (CL2, H2S, NH3, SO2, NOX etc.) ●High humidity place (ex. Kitchen, Bath room) ●In strong magnetic & electrical wave atmosphere (ex. Magnet, Display, Speaker, Radio etc.)
	Care should always be exercised when handling and operating this product with your equipment or device. **You are liable for the repair cost of damages or malfunctions caused by the following.** ●Do not drop or damage this product. ●Do not put things on this product. ●No food or drink beside this product. ●Do not put any materials or liquids on this product. ●Avoid any ingression of materials, metals or smoke into this product and its connector.
	Use the specified power cable connector and Camera Link™ cable.
	Power OFF when you insert or remove cables. Otherwise, an electric shock or a malfunction may occur.

1-2 PRECAUTIONS

	Caution
	**Keep this product clean. And do not touch the glass surface of this product.** Otherwise, a defect or a failure may occur. When you need to clean this product, you must clean the glass surface of this product with a soft cloth and IPA.
	**Put cables in a fixed position appropriately while operating.** Otherwise, a connection failure and damage may occur.
	**Do not use it in an unstable place such as on a wobbling table or on an inclined place.** This Product may fall and cause injury or malfunction.
	**Do not use or operate this product in a humid, smoky, vaporized or dusty place.**
	**Do not disassemble the side-bracket for mechanical mounting to your equipment or device.** Otherwise, an ingression of materials and dust, or a defect or a malfunction may occur.
	**Be cautious of your clothes and arms not to be caught by the sheet metal attached to the both side of this product.** It may cause injury.

1-2 PRECAUTIONS

	Caution (Disclaimer)
	Mitsubishi Electric assumes no responsibility and no liability for any damages resulting from a fire, earthquake or any other act of God, acts by third parties, misoperation by the user intentionally or accidentally, or used under extreme operating conditions.
	Mitsubishi Electric assumes no responsibility and no liability for any damages resulting from indirect, additional or consequential damages, including but not limited to loss of expected income and suspension of business activities.
	Mitsubishi Electric assumes no responsibility and no liability for any damages resulting from an unintended use as stipulated in Manual and Datasheet of this product.
	Mitsubishi Electric assumes no responsibility and no liability for any damages resulting from improper handling, use or repair by any party other than Mitsubishi Electric.
	Mitsubishi Electric warrants this product in conformity with the specification specified only in the Datasheet and the Manual of this product.
	Mitsubishi Electric's total liability shall not exceed the purchase price of this product.

1-2 PRECAUTIONS

	Handling precautions
	Handle this product carefully. Do not drop, shock, vibrate this product.
	Do not operate not in compliance with the conditions defined in the Datasheet and the Manual of this product.
	Keep this product cool with the appropriate thermal management referred to in "2-8 Handling precautions" if this product is used in no-air flow area.
	This product is designed as an embedded line camera module. Determine the applicability of this product to your equipment or devices through the appropriate analysis or evaluation by the designer of such equipment or devices, or personnel related to the specification. Such designers or personnel shall warrant the performance and safety of your equipment or devices such as dust-proofing, water-proofing, EMC and EMI, by themselves.

1-3 CE Marking

1-3-1 CE Mark compatibility conditions

KD6R309AX4, KD6R335AX4, KD6R617AX4, KD6R309AX4-NL, KD6R617AX4-NL are designed to comply with EMC Directive 2014/30/EC of EU legislation.

In order to make this product CE mark compliant, use this product under the following conditions.

1. Length of 5V and 24V power supply cables and Camera Link™ cables have to be 3m or shorter.
   Attach ferrite cores recommended in the following pages with the power supply cables and Camera Link™ cables in order to reduce noise emission.
   The details of the ferrite cores are explained in the following pages.
2. Prepare your power supply with surge suppression dedicated for this product, and supply 5V and 24V power to this product.

Moreover, this product is designed as an embedded module. When this product shall be installed to the other equipment, the equipment has to be compliant with the necessary regulation and directives.

This product is complied with the following EMC directives and standards.

EMC directives		2014/30/EC
Applicable standards:	Immunity	EN 61000-6-2:2005 + AC:2005
	Emission	EN 61000-6-4:2007 + A1:2011

Category of ISM equipment by EN55011: Comply with Group 1, Class A test standard.
Class A equipment is regulated to be used under industrial environment. It could be potentially difficult to assure the electromagnetic compatibility under other environments.
Refer to EN55011 standards for further details.

1-3 CE Marking

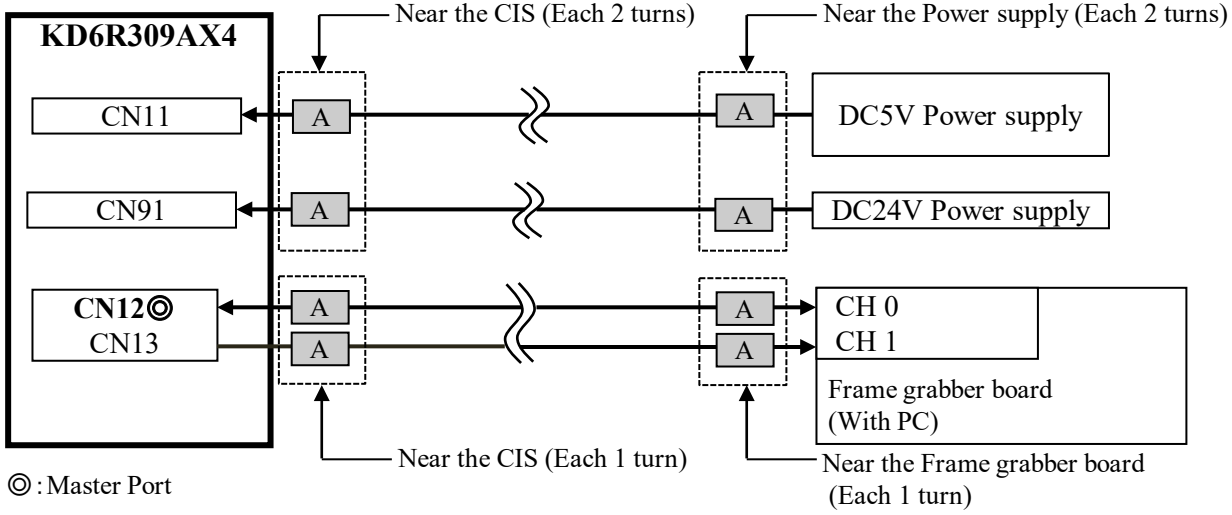
1-3-1 CE Mark compatibility conditions

1. KD6R309AX4（A3 type）

In order to make this product complied with CE mark, attach ferrite cores on the cables as shown on the left diagram. The ferrite cores enable to reduce the noise emission from the cables.

Recommended ferrite cores are shown below.
Ferrite core A : RFC-H13 KITAGAWA INDUSTRIES CO.,LTD
Frame grabber board : Matrox RAD EV 1G CLSF* or RAD EV 1G CLDF*

1. KD6R309AX4 (A3 type)
Attach ferrite cores as described in below.
- Cable between CN11 connector and 5V power supply : 2 Ferrite cores A (2 turn)
- Cables between Connector CN91 and illumination : 2 Ferrite cores A (2 turn)
- Cables between Connector CN12,CN13 and Frame grabber board : each 2 Ferrite cores A (1 turn)



1-3 CE Marking

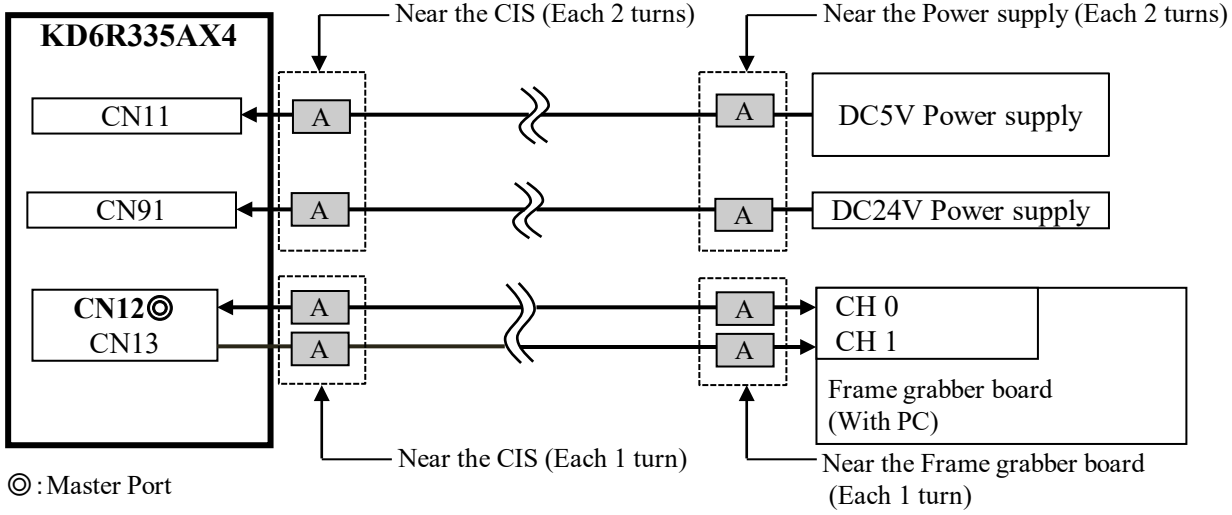
1-3-1 CE Mark compatibility conditions

2. KD6R335AX4（A3+(A3 nobi) type）

In order to make this product complied with CE mark, attach ferrite cores on the cables as shown on the left diagram. The ferrite cores enable to reduce the noise emission from the cables.

Recommended ferrite cores are shown below.
Ferrite core A : RFC-H13 KITAGAWA INDUSTRIES CO.,LTD
Frame grabber board : Matrox RAD EV 1G CLSF* or RAD EV 1G CLDF*

2. KD6R335AX4 (A3+(A3 nobi) type)
Attach ferrite cores as described in below.
- Cable between CN11 connector and 5V power supply : 2 Ferrite cores A (2 turn)
- Cables between Connector CN91 and illumination : 2 Ferrite cores A (2 turn)
- Cables between Connector CN12,CN13 and Frame grabber board : each 2 Ferrite cores A (1 turn)



1-3 CE Marking

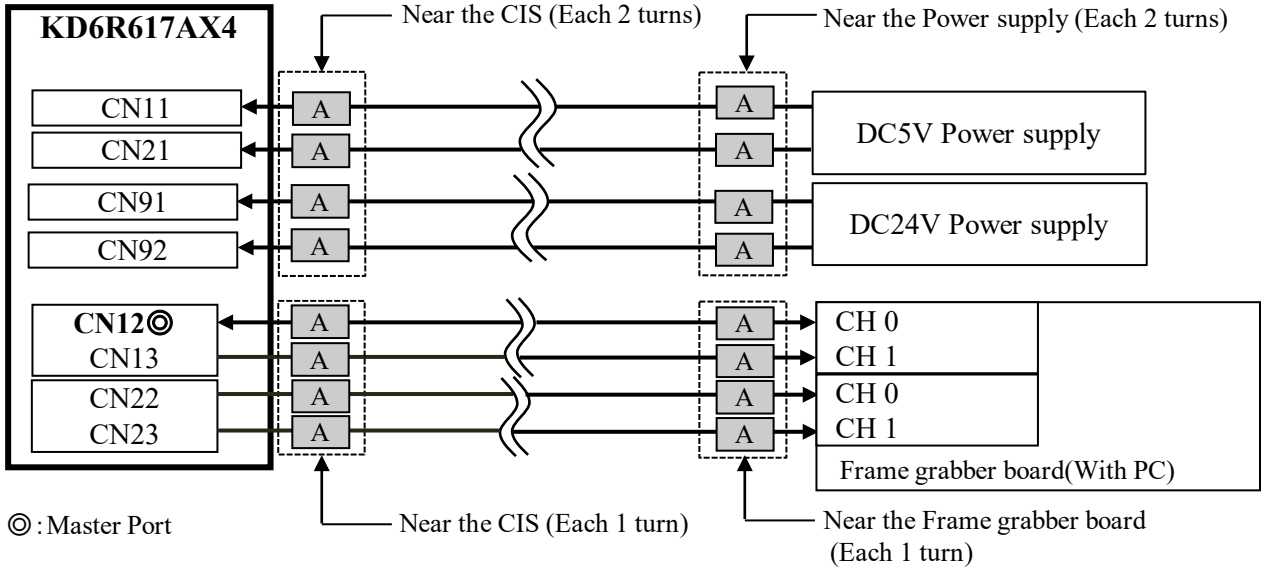
1-3-1 CE Mark compatibility conditions

3. KD6R617AX4（A1 type）

In order to make this product complied with CE mark, attach ferrite cores on the cables as shown on the left diagram. The ferrite cores enable to reduce the noise emission from the cables.

Recommended ferrite cores are shown below.
Ferrite core A: RFC-H13 KITAGAWA INDUSTRIES CO.,LTD
Frame grabber board : Matrox RAD EV 1G CLSF* or RAD EV 1G CLDF*

3. KD6R617AX4 (A1 type)
Attach ferrite cores as described in below.
- Cable between CN11,CN21 connector and 5V power supply : 2 Ferrite cores A (2 turn)
- Cables between Connector CN91,CN92 and illumination : 2 Ferrite cores A (2 turn)
- Cables between Connector CN12,CN13,CN22,CN23 and Frame grabber board : each 2 Ferrite cores A (1 turn)



1-3 CE Marking

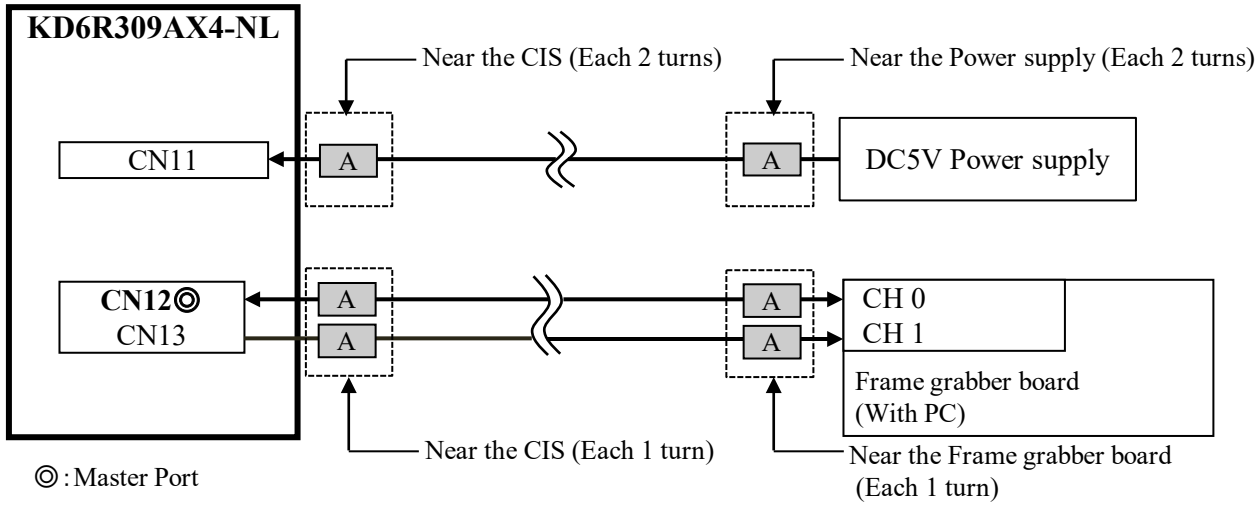
1-3-1 CE Mark compatibility conditions

4. KD6R309AX4-NL
（A3 type Non-Illumination Model）

In order to make this product complied with CE mark, attach ferrite cores on the cables as shown on the left diagram. The ferrite cores enable to reduce the noise emission from the cables.

Recommended ferrite cores are shown below.
Ferrite core A : RFC-H13 KITAGAWA INDUSTRIES CO.,LTD
Frame grabber board : Matrox RAD EV 1G CLSF* or RAD EV 1G CLDF*

4. KD6R309AX4-NL (A3 type Non-Illumination Model)
Attach ferrite cores as described in below.
- Cable between CN11 connector and 5V power supply : 2 Ferrite cores A (2 turn)
- Cables between Connector CN12,CN13 and Frame grabber board : each 2 Ferrite cores A (1 turn)



1-3 CE Marking

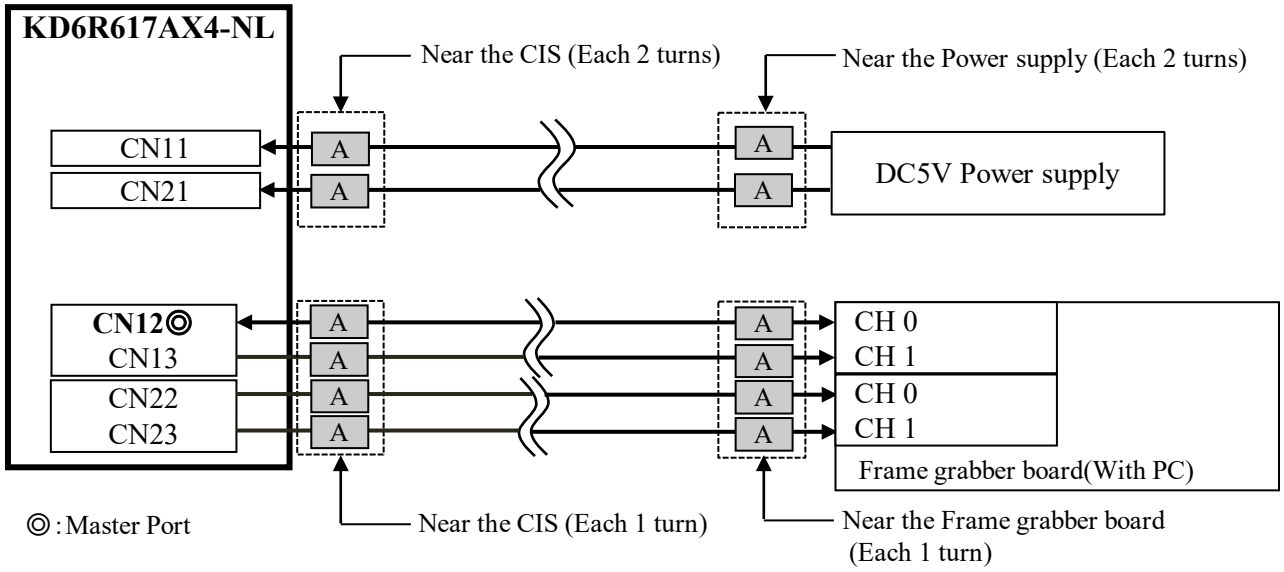
1-3-1 CE Mark compatibility conditions

5. KD6R617AX4-NL
（A1 type Non-Illumination Model）

In order to make this product complied with CE mark, attach ferrite cores on the cables as shown on the left diagram. The ferrite cores enable to reduce the noise emission from the cables.

Recommended ferrite cores are shown below.
Ferrite core A : RFC-H13 KITAGAWA INDUSTRIES CO.,LTD
Frame grabber board : Matrox RAD EV 1G CLSF* or RAD EV 1G CLDF*

5. KD6R617AX4-NL (A1 type Non-Illumination Model)
Attach ferrite cores as described in below.
- Cable between CN11,CN21 connector and 5V power supply : 2 Ferrite cores A (2 turn)
- Cables between Connector CN12,CN13,CN22,CN23 and Frame grabber board : each 2 Ferrite cores A (1 turn)



1-4 WARRANTY

1-4-1 Warranty

Mitsubishi Electric warrants this product in conformity with the specification specified only in Datasheet and Manual of this product within warranty period.
(Mitsubishi Electric does not warrant any devices, equipment, and systems, which comprise this product.)

1-4-2 Warranty period

1 year from the factory shipment date.

1-4-3 Contents of warranty

If any product failure or defect which is recognized to happen under Mitsubishi Electric's responsibility is found within the warranty period, any repair services at Mitsubishi Electric's own expense or replacements with the same product under the scope of product specification shall be provided.

1-4-4 Out of Warranty

Notwithstanding above, this product shall not be warranted in the following circumstances.

- In case of out of warranty period.
- In case of improper handling, use or repair by any other party than Mitsubishi Electric.
- In case of improper conditions that are not stipulated in the data sheet or the manual and damage this product by direct sunlight, water, any chemicals, external pressure, etc.
- In case of a malfunction due to improper use.

The cost of repair or replacement shall be charged to the customer who requested to repair the out of warranty product. Also, Mitsubishi Electric shall not be liable to any indirect damages, consequential damages, etc. related to the product.

1-5 REPAIR

1-5-1 Repair method

Your sole remedy shall be repair or replacement of this product (Contact Image Sensor), provided that the defective product is returned to our factory and analyzed by Mitsubishi Electric.
When you return this product (Contact Image Sensor) to Mitsubishi Electric, return it according to the packing specification of the shipment and use our packing materials (refer to 2-6 Packaging). If you cannot use our packing materials, this product should be protected by more than triple bubble wrap and be put it on suitable case.

Notwithstanding above, depending on circumstances of the discontinuity of material procurement and facility, repair of this product may not be available. In that case, such request is handled as an upgrade or repair into other equivalent products.

1-5-2 Request of repair

If you need to return this product for repair, you must contact the agency who sold you this product. Do not return your product to Mitsubishi Electric without prior authorization.
The shipment cost to return this product shall be borne by sending party.

1-5-3 Repair period

This product would be repaired for 1 year after the final production of this product, provided that Mitsubishi Electric would be able to maintain production equipment or tools and procure the necessary materials for the repair. The prior announcement of the discontinuation of this product will be announced through the agency who sold you this product, or through our website.
Please note that we may send you a replacement if the product can’t be repaired.

MITSUBISHI ELECTRIC
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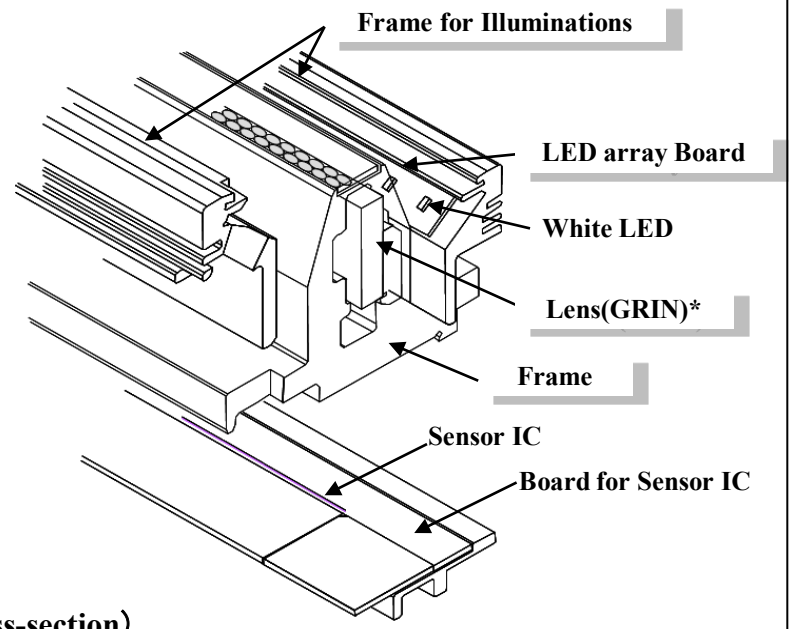
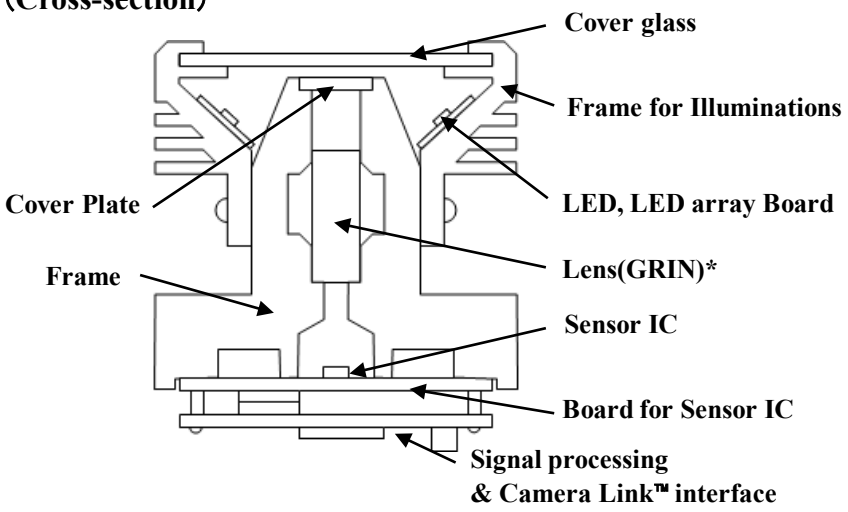
Chapter 2 : Overview

2-1 What's Contact Image Sensor

(Perspective view)



(Cross-section)



This product (CIS : Contact Image Sensor) is a scanning device that comprises several key-components as follows;

- Sensor IC array in the length as same as scan width.
- Rod lens array in the length as same as scan width.
- Illumination in the length as same as scan width.

*GRIN lens : Gradient Index lens

The features of CIS can be compared to line camera as follows;

	CIS	Optical reduction system
1. Resolution	Fixed	Flexible
2. Depth of focus	Shallow (±0.5～ 2mm)	Deep (～ over 4mm)
3. Distortion	Small	Large
4. Light path	Short (10～50mm)	Long(～200mm)
5. Requested light intensity	Small	Large
6. Power consumption	Small	Large
7. light-sensitive element	CMOS / CCD	CMOS / CCD
8. Impacting and vibration	Strong	Weak
9. Setup adjustment	Easy	Need to be adjusted with lens precisely.
10. Outline	Compact	Large

2-2 Principal technology of CIS

(How to acquire reflective light)

Fig.1

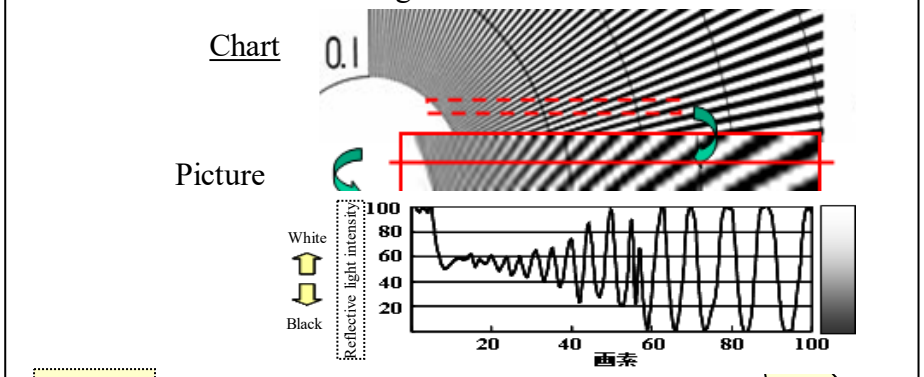


Fig.2

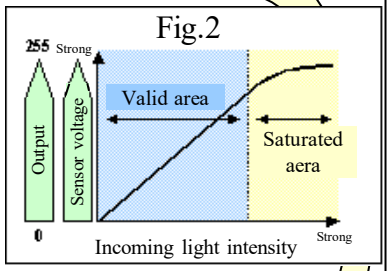
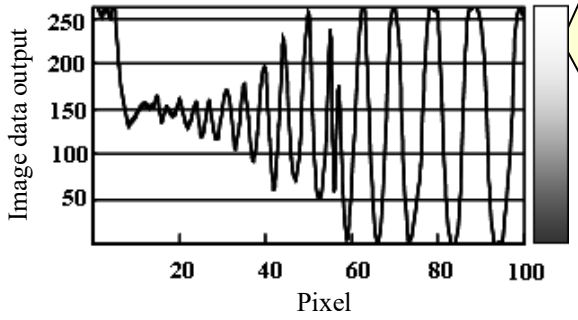


Fig.3



This clause explains how to acquire the raw information of the light and convert into electrical signal information.

・When scanning a surface of the object, the illumination on this product irradiates the object.

・The object reflects the light. Generally, the illuminated black object reflects weaker reflective light. On the other hand, the illuminated white object reflects stronger one.

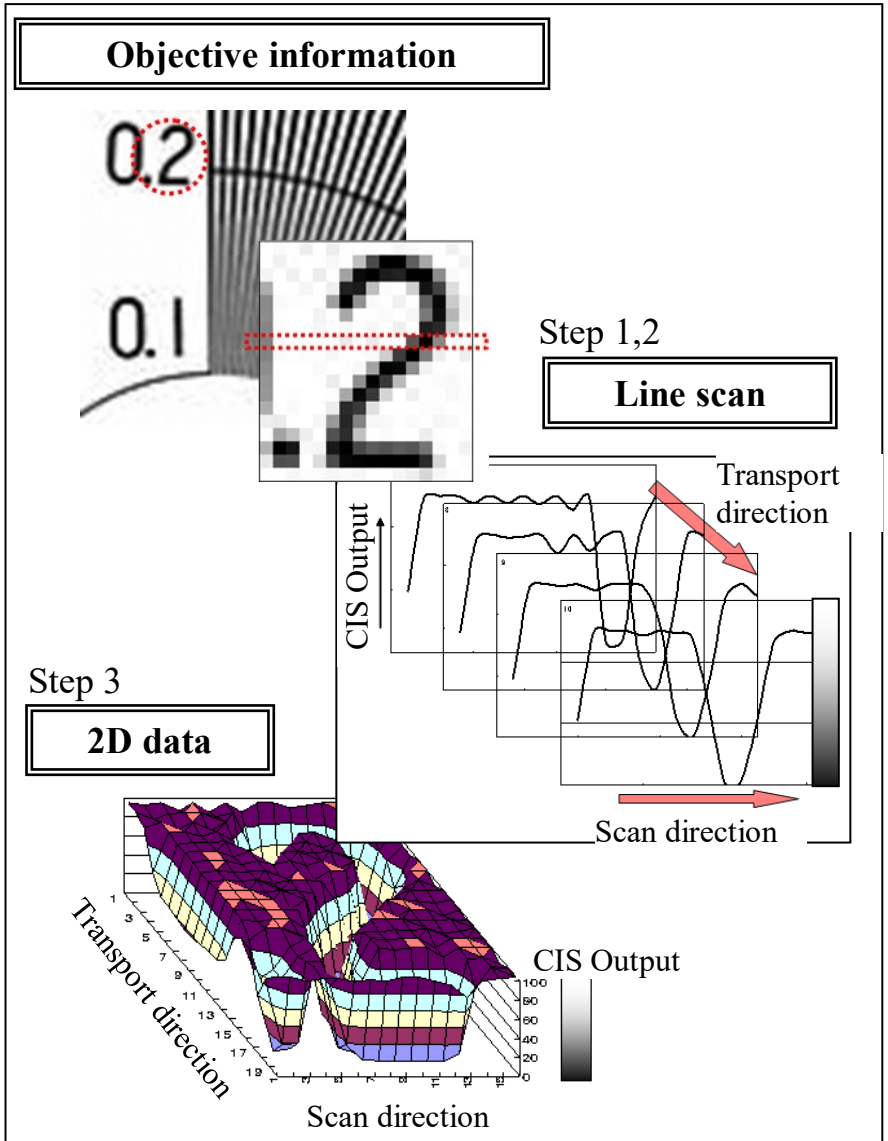
・Refer to the drawing on left side (Fig.1). The black and white charts have a correlation with the reflected light intensity.

・The strong and weak reflective light arrives at the surface of Sensor ICs (photo-diodes) through lens.

・As described in the drawing on the left side (Fig.3), Sensor ICs correspondingly convert the strong and weak light into the large and small electrical signal based on the converting property of Sensor ICs as described on the drawing on left side (Fig.2).

・Sensor ICs are arranged in an array and detect the optical information corresponding to that position.

2-2 Principal technology of CIS



This product captures 2D image by scanning one line repeatedly and continuously.

・Acquiring a data of one line in scan direction.

・Relative transport in transport direction between the object and this product can accumulate 2D data.

Refer to left side of the drawings.

【Example of scanning “2”】

・Step 1: Sensor IC reads one line in red point-line area. The size of the line in transport direction is based on the size of pixel.

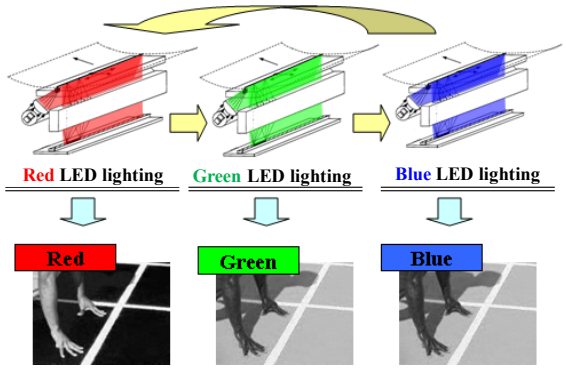
・Step 2: The scanning line is transported in transport direction.

・Step 3: Repeating Step 1 and 2 generates 2D image data. (The height of the 2D-data means the strength of CIS output.)

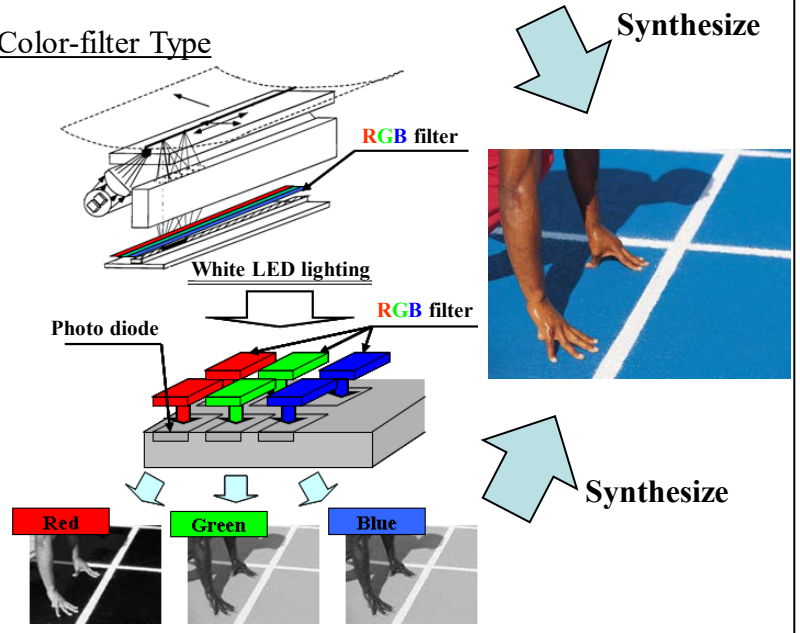
2-2 Principal technology of CIS

(Color scanning method)

1. Sequential lighting Type



2. Color-filter Type



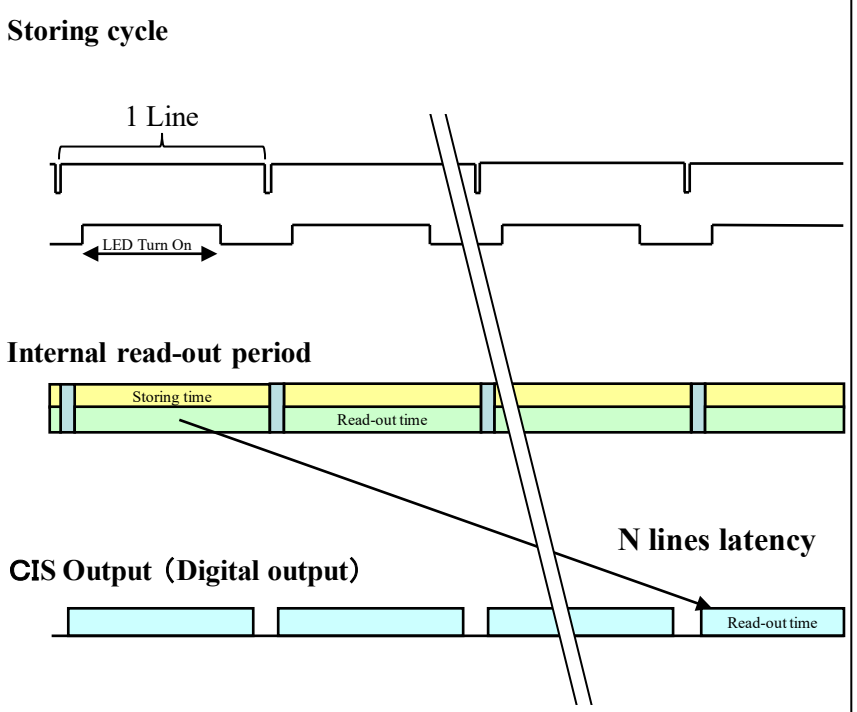
(Color scanning method)

Principally, there are two ways to scan color image.
1. Sequential lighting Type
2. Color-filter Type

This product takes “ 2. Color-filter Type” above for the color scanning method. And it has a color Sensor IC array based on trilinear photo-diode with RGB color filters. Utilizing this filter-on-chip technology, this product can get a color image data in a respective storing time.

2-2 Principal technology of CIS

(Data output timing)



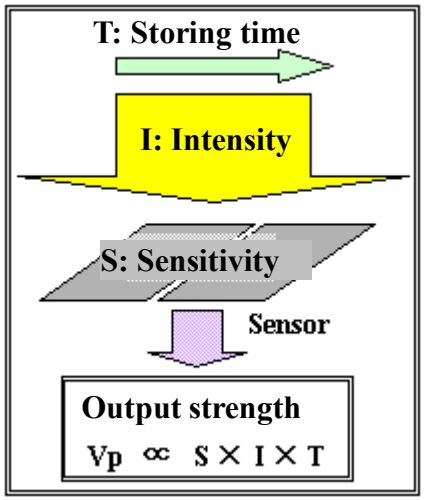
(Data output timing)

There is a latency to read-out a line data. The N lines latency is designated from LED turn ON as described on the left drawing.

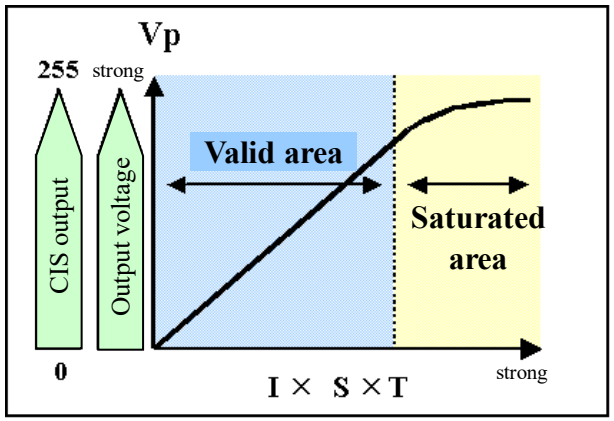
1) Sensor converts the information by light into the information by electric (1 line)
2) Period to read out the analog data of sensor pixels (1 line)
3) Period to convert the analog data into digital data and rearrange the data in a line (1 line)
4) Period to process internal image processing (N lines latency : about 3 lines ~10 lines)

2-2 Principal technology of CIS

(Strength of Sensor IC output)



(Property of Sensor IC)



(CIS output)

CIS output (Vp) is defined below;

- Light intensity : I
- Sensor IC Sensitivity : S
- Storing time (illuminated time to Sensor IC) : T

$$Vp = k \times I \times S \times T$$

(k: coefficient)

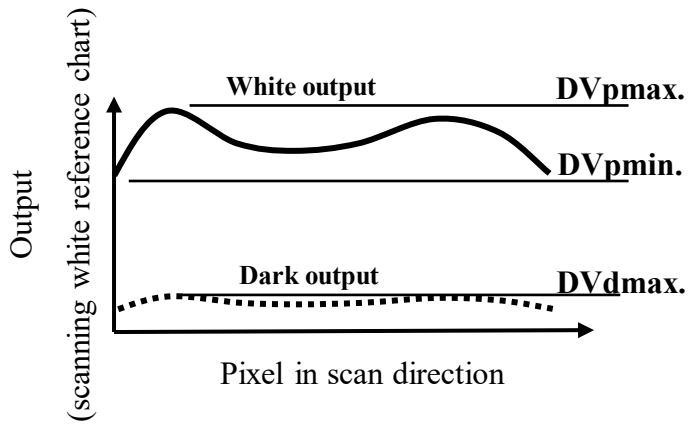
(Remark)

1) To keep a quality of the image, Vp is an important factor so that Light intensity (I) and Storing time (T) have to be adjusted appropriately.

2) If the intensity of the light source becomes too strong, CIS output will be saturated. In order to avoid such a saturation of the output, adjust the illumination's intensity (illumination-duty) appropriately.

2-3 Definition

(White output and Dark output uniformity)



(Definition of CIS output)

This product comprises CMOS sensor IC which each pixel has each DC offset and variation of sensitivity. And the variation of lens and light intensity also affects the CIS output. CIS output is as defined below.

1. Dark output uniformity
Dark output uniformity is an output uniformity when the illumination is turned OFF.
Dark output is defined as maximum value DVd max.

2. White output uniformity
White output after Dark correction (DVEp) means white output value after subtracting dark output from sensor output pixel by pixel . DVEp is calculated as follows;

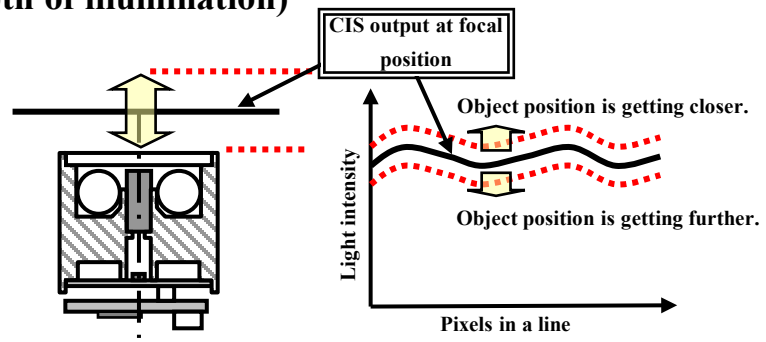
$$DVEp(n) = DVp(n) - DVd0(n).$$

White output uniformity (UEp) indicates the output variation which occurs when this product is scanning white reference chart. White output uniformity is calculated as follows;

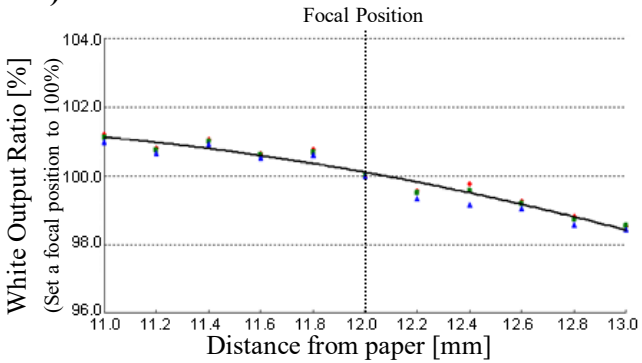
$$UEp = (DVEp\ max.- DVEp\ min.)／DVEp\ max.$$

2-3 Definition

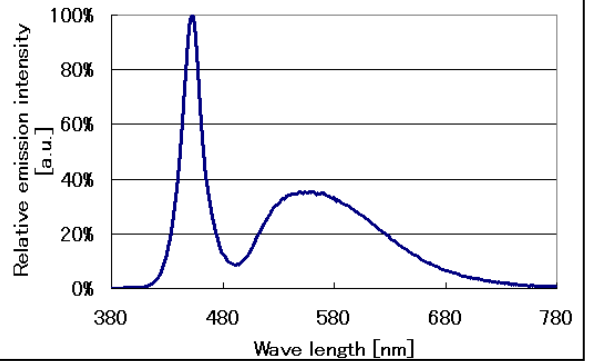
(Depth of illumination)



(DOI of KD series)



(Spectrum of illumination)



(Definition of CIS output)

3. Light intensity
This indicates a strength or intensity of the light on a surface of the object. As described on the left, CIS output Vp is controlled by "Light intensity (I)" * "Storing time (T)". Therefore, in order to increase scanning speed, Light intensity also needs to be increased.

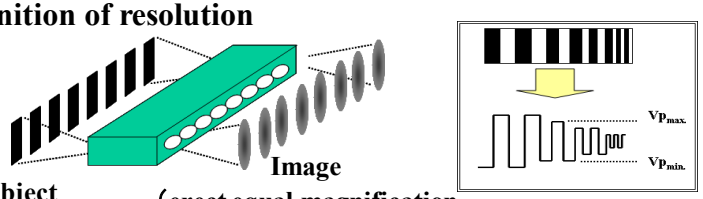
4. DOI : Depth of Illumination
Depth of Illumination indicates a variation of a light intensity on various positions of the object in lens-axis direction.
Generally, CIS output would be getting increased when the scanning position comes closer to this product. By contrast, CIS output would be getting decreased when the scanning position goes further from this product.
Larger variation of DOI would make a difficulty to detect whether that the output variation is caused by reflectance of the
object or position of the object.

5. Spectrum of illumination
This product comprises white LED array as a built-in illumination. Refer to the spectrum of illumination on the left.

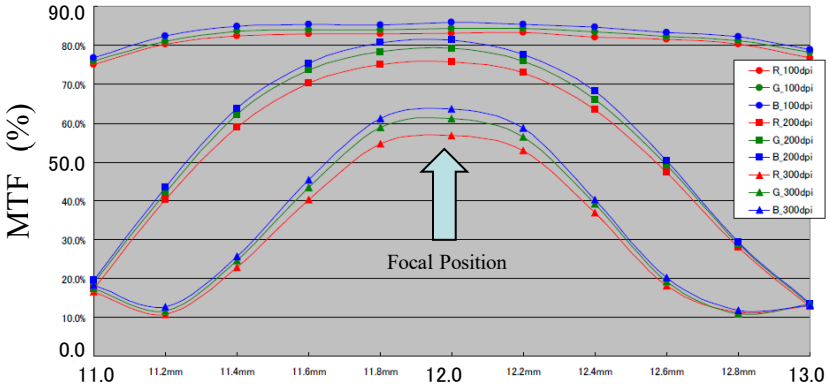
2-3 Definition

(Depth of Focus)

Definition of resolution



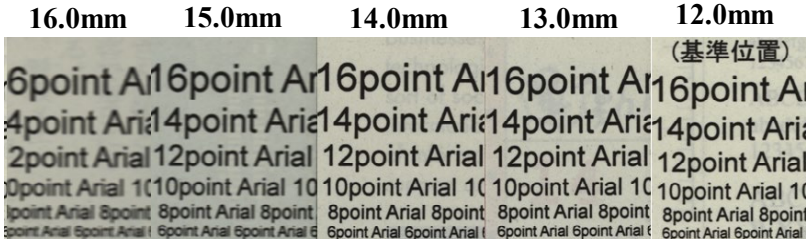
Example . Depth of Focus on KD series



Position from the Cover glass (mm)

(Caution)The above figure doesn't guarantee the absolute value.
It is a diagram showing that there is a similar tendency

Scan images



(Definition of CIS output)

6. DOF : Depth of Focus

Shows the change in resolution depending on the position of the scanning object.

Depth of Focus indicates a variation of a resolution on various positions of the object in a lens-axis direction. Generally, the resolution is getting defocused when the scanning position is moved away from a focal point.

The resolution is defined as MTF (Modulation Transfer Function) value.

The MTF value is calculated by the following formula when scanning a reference chart having a respective width and pitch of the white and black areas.

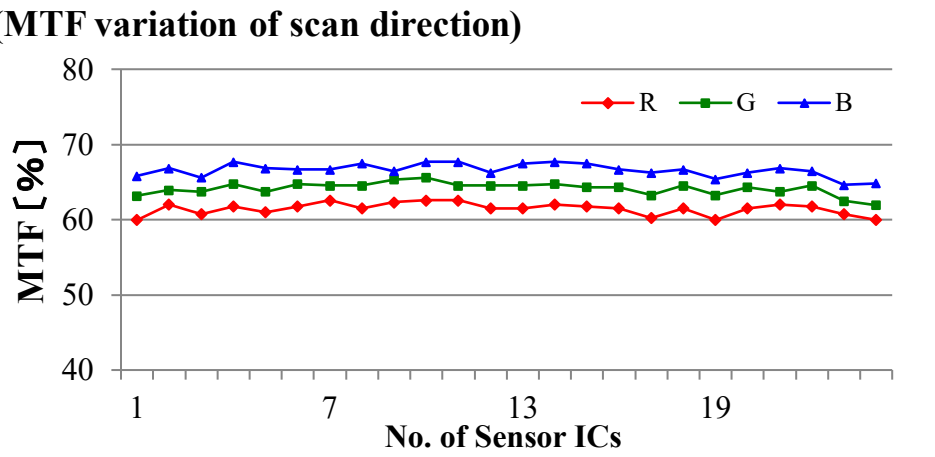
$$\mathbf{MTF} = \frac{\mathbf{DVEp\ max.} - \mathbf{DVEp\ min.}}{\mathbf{DVEp\ max.} + \mathbf{DVEp\ min.}} \times \mathbf{100}\ \mathbf{(\%)}$$

lp/inch: This product's resolution can be grasped by scanning a chart in which black lines and white lines of the same thickness are arranged alternately. This pair of black and white lines is called a line pair, and lp / inch indicates how many pairs of line pair = lp are printed on 1 inch.

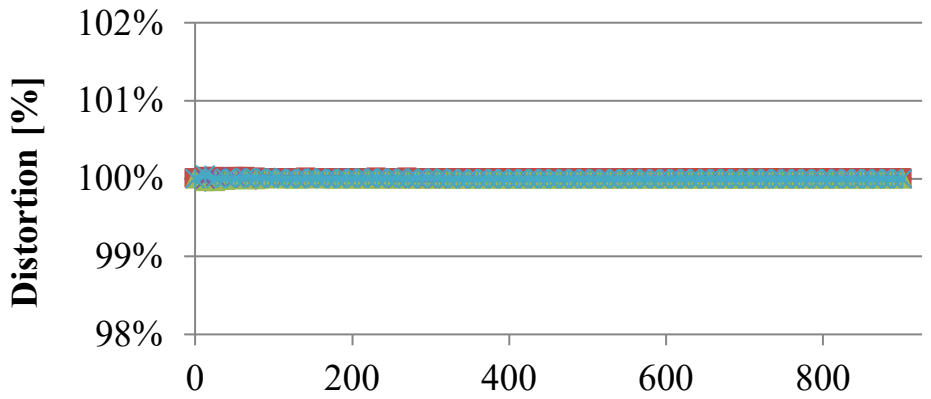
For example, 150 lp / inch means that 150 pairs of black and white lines are arranged alternately in 1 inch.

Represents a chart with 25.4 / 300 = 84.66, that is, a line about 85 μm wide printed.

2-3 Definition



Variation of MTF (example)（KD6R309AX4：A3Size)



Distortion ratio of KD Series

(MTF variation of scan direction)

The graph on the left shows a property of resolution uniformity in the scanning direction of KD6R1064DXL-NL. Each dot on this Graph shows MTF value of each sensor chip in a CIS.

1. MTF value variation in the scanning direction
The graph on the upper left shows an example of MTF values of each sensor ICs. This shows that this CIS has uniform resolution in whole scanning width.

2. Distortion
The graph on the lower left shows an example of distortion values in 1st pixel of each sensor ICs, which are calculated by measurement value of each pixel after assemble (n = 5).

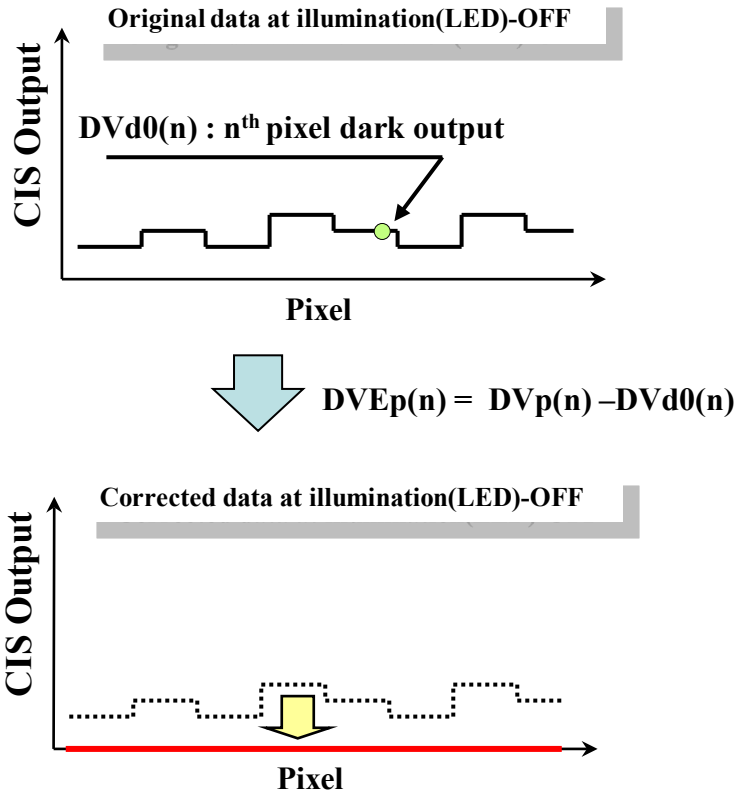
Distortion(%)
= Measured distance*1 / Designed distance*2 × 100

*1 Measured distance: a distance between the first pixel and the measured pixel.
*2 Designed distance: an ideal distance between the first pixel and the designed pixel.

This data shows that this CIS has extremely less distortion in whole scanning width.

2-3 Definition

(Function of Dark correction)



(CIS output and signal processing function)

This product is equipped with correction functions of the pixel unit. These functions correct the variations due to DC offset and the sensitivity variation of each pixel of the CMOS sensor, the lens, and the illuminations, and enable this product to provide good images.

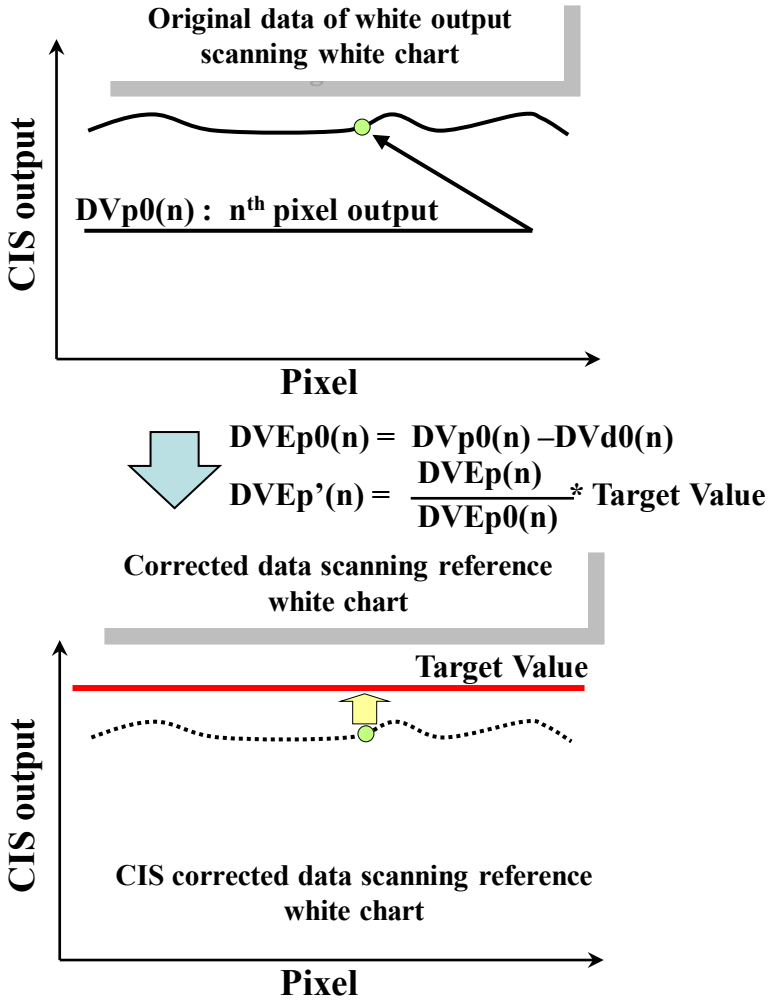
1. Dark correction

This is a function that corrects DC-offset on each pixel into zero. This function subtracts the pixel dark-correction data (Dvd0 (n)) from the original pixel dark output data (Dvp (n)) pixel by pixel.

Dark-correction data (Dvd0 (n)) is generated by averaging 32 lines of the data to minimize the effect of noise on each pixel in the condition of turning off the illumination. Using Dark correction on CIS output allows this product to provide the only dynamic range responding the incoming light.

2-3 Definition

(Function of White correction)



(CIS output and signal processing function)

2. White correction

CIS output corrected by Dark correction is affected by the sensitivity of the CMOS sensor, the imaging efficiency of the lens, and the illumination intensity. White correction enables this product to correct these variations and to provide a uniform output, when a uniform-reflectance chart is scanned.

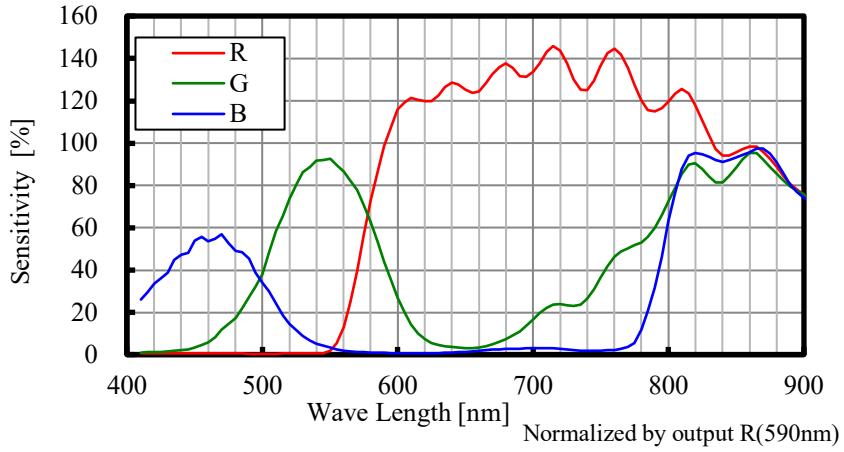
White correction corrects the white output (DVEp (n)) acquired in an actual scanning operation by using the white correction data (DVEp0(n)) acquired in scanning another object having an uniform reflectance.
CIS output corrected by White correction, DVp'(n) is calculated by the following formula.

$$DVEp'(n) = \frac{DVEp(n)}{DVEp0(n)} * \text{Target Value}$$

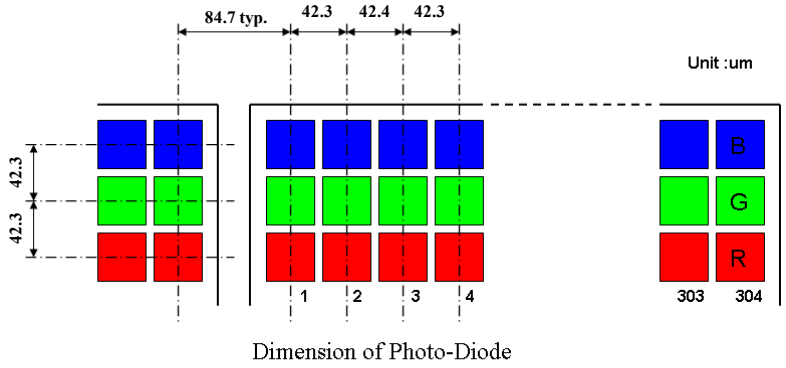
Target value can be set by register value.
There are several methods to create White correction data. Refer to Function specification for further detailed information.

2-4 Features of scanning pixels

(Sensor IC spectral sensitivity)



(Pixel alignment of Sensor ICs)



Dimension of Photo-Diode

(Sensor IC spectral sensitivity)

This product comprises a color trilinear sensor ICs that feature Filter-on-Chip technology. The Sensor IC's spectral sensitivity is described on the left.

(Pixel alignment of Sensor ICs)

The plural Sensor ICs are assembled in a line on a sensor board in this product. The number of 288 pixels x 3 color Sensor ICs for each length are as follows;

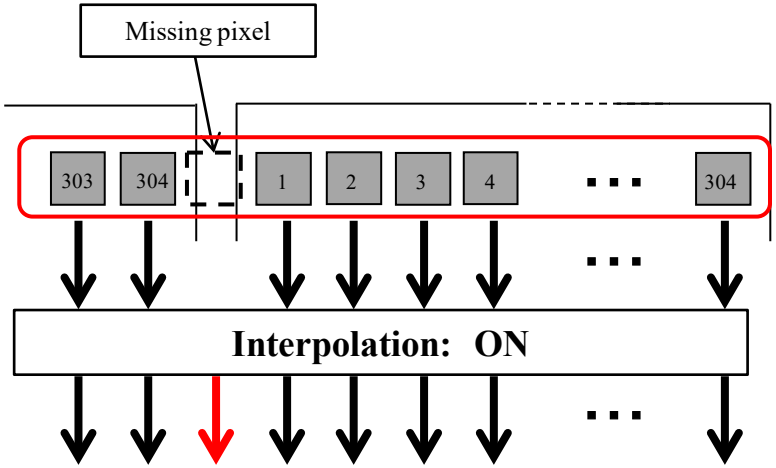
300 mm size : 24 chips
600 mm size : 48 chips
900 mm size : 72chips

The resolution between the neighboring pixels of neighboring Sensor ICs is not 600 dpi, and is designated to be 300 dpi (84μm) pitch and controlled to be placed within 1/3 pixels(±about 15μm) tolerance, because keeping enough dicing area at the edge of Sensor ICs is necessary.
Therefore, the pixel pitch between the neighboring sensor ICs is arranged in 300dpi pitch, and doesn't output a pixel data between sensor ICs, which is called "missing pixel".

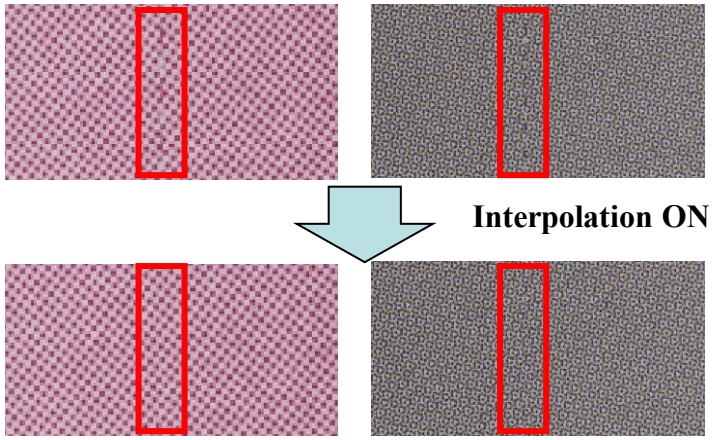
Additionally, a function of Interpolation that can insert a pixel data created by neighboring pixels data for each gap between neighboring Sensor ICs is available on this product.

2-5 Interpolation function 1 (Interpolation between chips)

(Conceptual Diagram of Interpolation)



(Interpolation example)



【Interpolation function】

This product has a Sensor IC array having a reduction of a resolution at the gap between sensor ICs. This is a function to compensate a reduction of the resolution between neighboring Sensor ICs.

【Technology of Interpolation】

To get the most expected Interpolation data, the resolution of the gaps between neighboring Sensor ICs are designated to be 300dpi and precisely controlled by the tolerance of ±about 15μm in X/Y direction.

The missing pixel data can be generally interpolated by generating the data of missing pixel based on Filter Interpolation.

If the image data is cyclic, the missing pixel data may need to be interpolated by generating the data of missing pixel based on "Average keeping interpolation". Refer to the following patent publication for further detail.

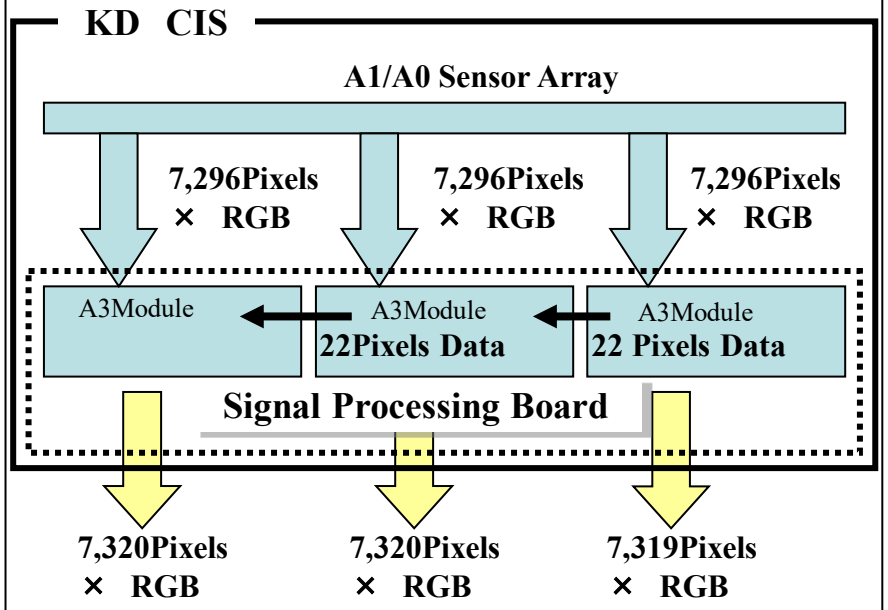
Japanese Related Patent No.:

(1) JP3767593B2
(2) JP3810404B2
(3) JP4199784B2
(4) JP4772754B2

2-5 Interpolation function 2 (Interpolation between A3 units)

(Interpolation in 926mm(A0)/617mm(A1) size)

Interpolated pixels are generated from 22 pixels data.



(Interpolation in 926mm(A0)/617mm(A1) size)

This product outputs the image data from each 309mm-size-unit (A3-size). In the case of 926mm-size (A0-size), there are 3 unites of 309mm-size (A3-size). And in the other case of 617mm-size (A1-size), there are 2 unites of 309mm-size (A3-size).

Interpolation on 926mm (A0) and 617mm (A1) size creates the interpolated pixel data between each unit.
(Neighboring 309mm-size-unit (A3) communicates and transfer 22 pixels data as described on the left and can create the interpolated pixels between each 309mm-size-unit (A3).)

The pixel data created by Interpolation is inserted as;
・the last pixel data of the first 309mm (A3) size unit in 617mm-size (A1) product.
・ the last pixel data of the first and second unit (A3) in 926mm-size (A0) product.

2-6 Overlap output function

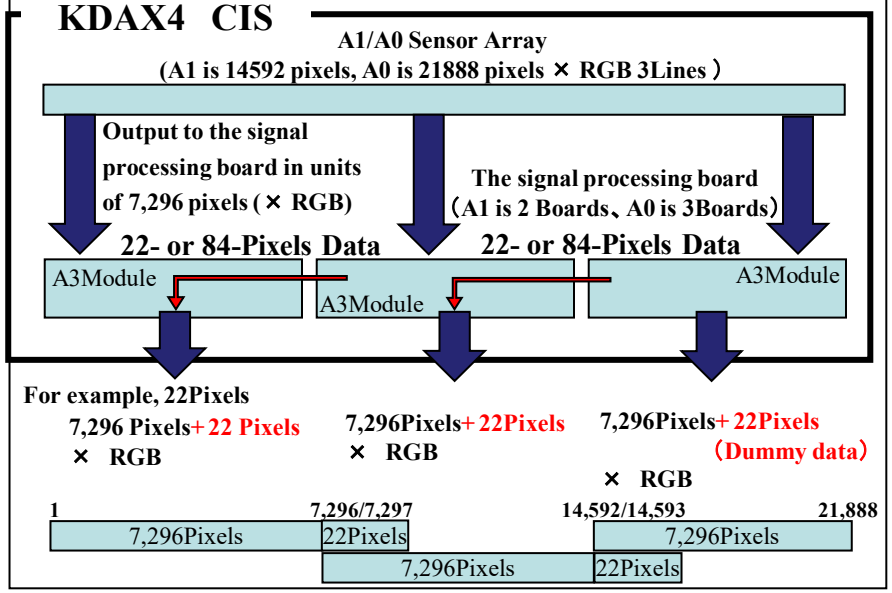
(Overview of overlap function)

By enabling the overlap function, the data of the first 22 pixels or the first 84 pixels of the next module are added after the previous module.

By using the overlap function, it is easier to recognize the image near the boundary between A3 modules.

In the interpolation, one pixel generated from the first 22 pixels of the next module is added to the missing pixel between the sensor ICs. On the other hand, in the overlap, all pixel of 22 pixels or 84 pixels are added to the back of the A3 module.

The number for output pixels of the overlap function (Conceptual diagram)



(Description of overlap function)

The output of image data of this product is in A3 size units, and by overlapping the images between A3 modules, it is easier to recognize the image near the boundary.

This function can be used with A1 and A0 size products, and images are overlapped at the joints of A3 size modules. (Pixel data is exchanged between adjacent modules of A3 unit to generate an overlapping image.)

The pixels used for the Overlap function can be selected from 22 pixels data or 84 pixels data in the register.

For details, refer to 5-2 Setting 11: Overlap output setting in this document.

Pixels generated by the overlap function are output as follows.

-A1 size overlap pixels are output as the end side's pixel in the A3 module on the first pixel side.

-A0 size overlap pixels are output as the end side's pixel of each of the 1st and 2nd A3 modules on the first pixel side.

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2-7 Specifications

Please check the detailed specifications in the individual Datasheet.
The specifications of this product are subject to change without notice.

Item	Unit	A3:KD6R309AX4 A1:KD6R617AX4 A0:KD6R926AX4 A3+:KD6R335AX4	A3:KD6R309AX4-NL A1:KD6R617AX4-NL A0:KD6R926AX4-NL
Scanning width	mm	309.7 / 619.7 / 929.6 / 335.6	309.7 / 619.7 / 929.6
Number of Valid pixels	pixel	7,296 /14,592 / 21,888 / 7904 × R/G/B 3Line (Color)	7,296 /14,592 / 21,888 × R/G/B 3Line (Color)
Resolution	dpi (Dot per Inch)	600	600
Line scan frequency	kHz	(Other than KD6R335AX4) 22.7*1 / 11*2 (Max.) (Only KD6R335AX4) 20.7*1 / 10*2 (Max.)	22.7*1 / 11*2 (Max.)
I/F Format	–	Camera Link™	Camera Link™
Number of output ports	–	1 / 2 / 3*3	1 / 2 / 3 *3
Output Camera Link™ frequency (Output pixel clock)	MHz	84 max.	84 max.
Additional Signal Processing	–	1. White or Dark Correction 2. Pixel offset setting 3. Control of the LED illuminations 4. PGA 5. Interpolation , Overlap function 6. Gamma correction 7. Status LED display of operating status, etc. 8. Register setting AX3 compatibility mode	1. White or Dark Correction 2. Pixel offset setting 3. PGA 4. Interpolation , Overlap function 5. Gamma correction 6. Status LED display of operating status, etc. 7. Register setting AX3 compatibility mode
Illumination	–	White LED Array	No Illuminations
Focal position	mm	12.0	14.5
Outline (Center) (L × W × H)	mm	377 / 688 / 997 / 377 × 62 × 71	377 / 688 / 997 × 62 × 67
Weight	kg	1.7 / 3.1 / 4.5 / 1.7	1.2 / 2.2 / 3.1

 * 1 to 3 are explained on the next page.

2-7 Specifications

***1 , 2 The scanning speed depends on the data output format, output Camera Link™ frequency, and output resolution.**

The following are under the condition that output Camera Link™ frequency (output pixel clock) 84MHz and output resolution 600dpi are applied.

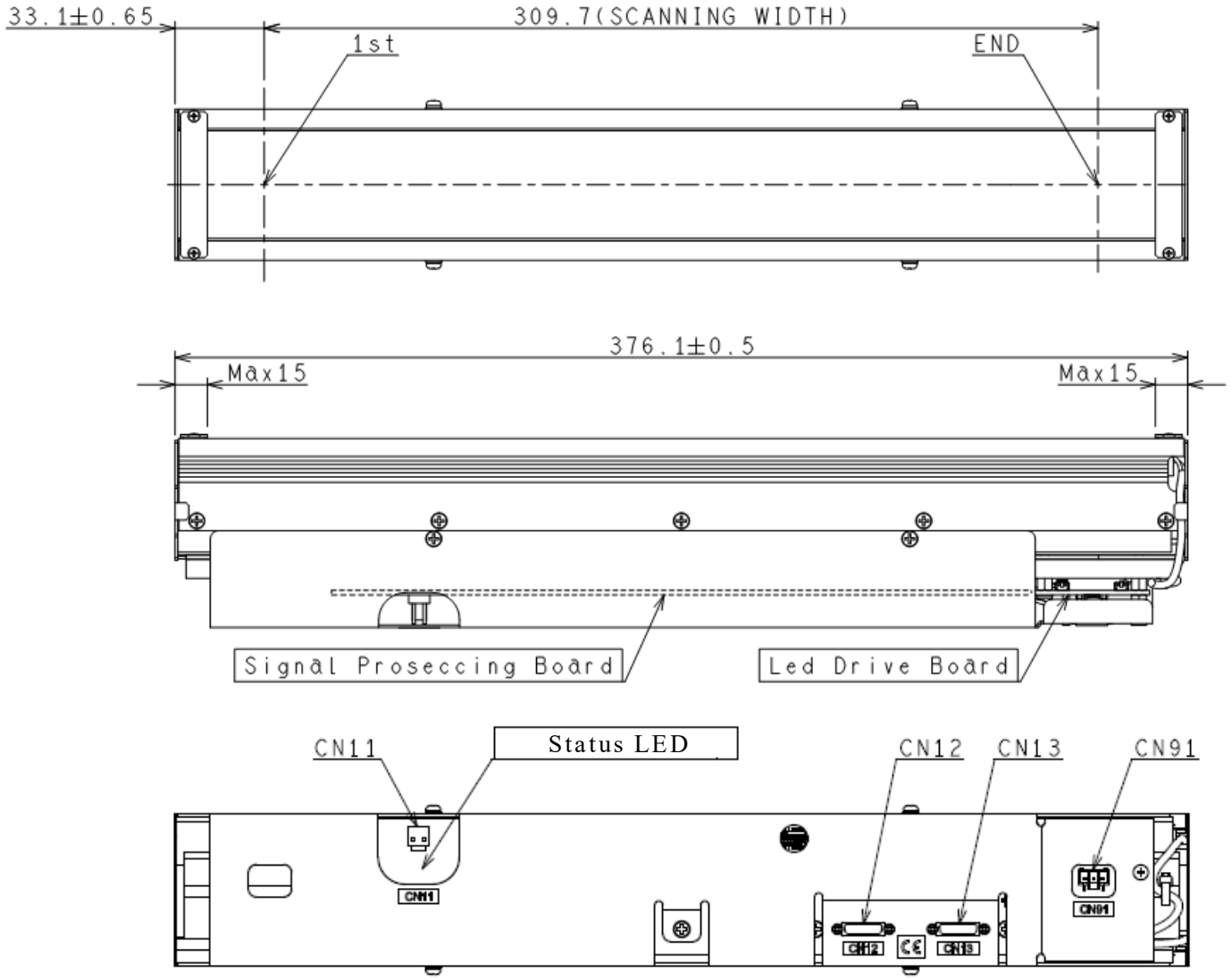
Camera Link™ Configuration	Format	Line scan frequency (kHz)	Storing time (µsec / Line)
Medium Configuration	8bit RGB Color 2Tap	(Other than KD6R335AX4) 22.7 (Interpolation OFF) 22.2 (Interpolation ON) (Only KD6R335AXA) 20.8 (Interpolation ON / OFF common condition)	(Other than KD6R335AX4) 44 (Interpolation OFF) 45 (Interpolation ON) (Only KD6R335AXA) 48 (Interpolation ON / OFF common condition)
Base Configuration 1	8bit RGB Color 1Tap	(Other than KD6R335AX4) 11 (Interpolation ON / OFF common condition) (Only KD6R335AXA) 10 (Interpolation ON / OFF common condition)	(Other than KD6R335AX4) 88 (Interpolation ON / OFF common condition) (Only KD6R335AXA) 96 (Interpolation ON / OFF common condition)
Base Configuration 2	8bit RGB Color 1Tap x 2 The same image of 8bit RGB color 1Tap output from two connectors.		
Medium Configuration	10bit RGB Color 1Tap		

***3 The signal output to be used for each output port is as follows.**

Camera Link™ Configuration	Format	Number of output channels
Medium Configuration	8bit RGB Color 2Tap	2 x Number of output ports
Base Configuration 1	8bit RGB Color 1Tap	1 x Number of output ports
Base Configuration 2	8bit RGB Color 1Tap x 2 The same image of 8bit RGB color 1Tap output from two connectors.	2 x Number of output ports
Medium Configuration	10bit RGB Color 1Tap	

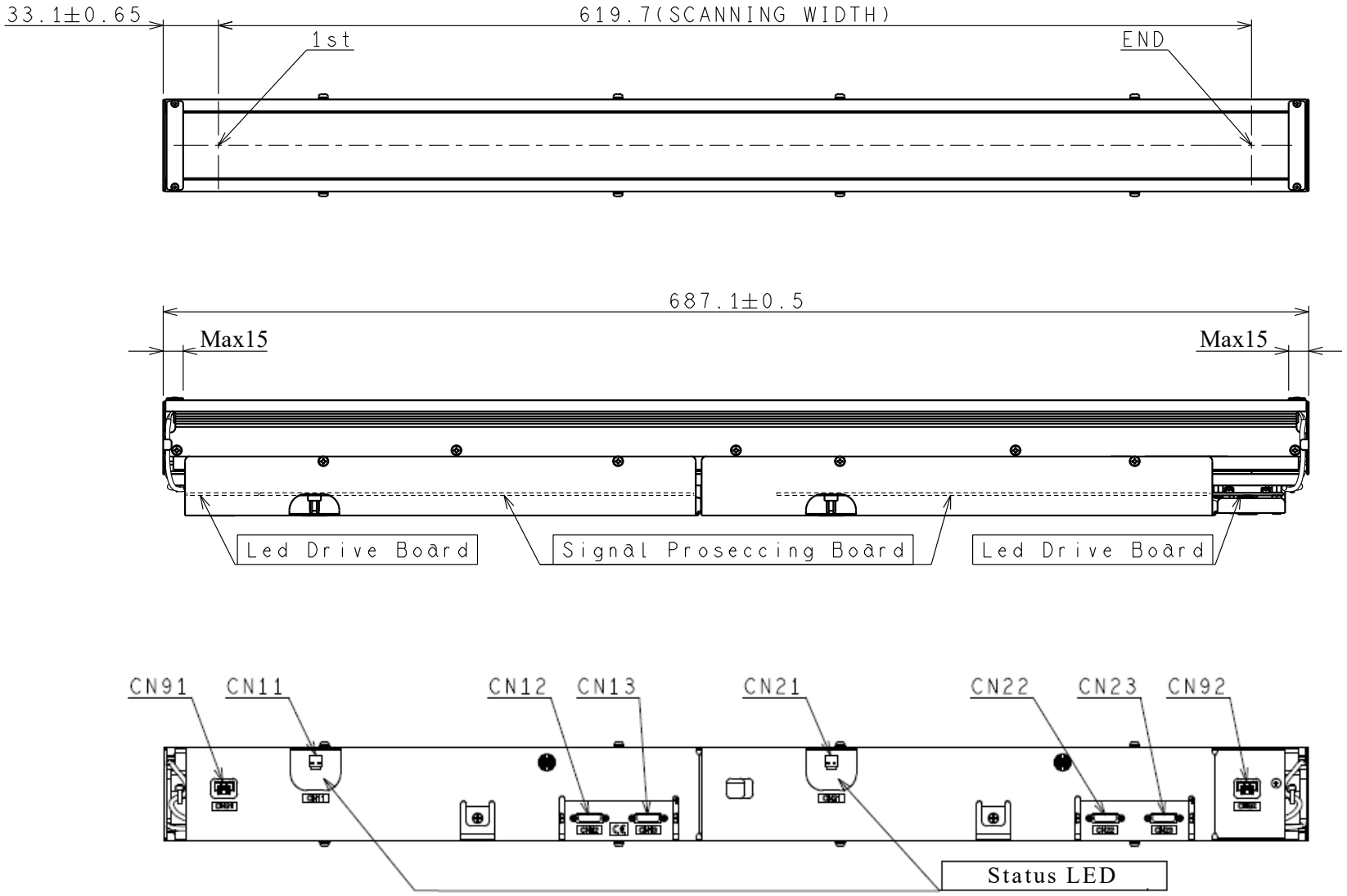
2-7 Specifications

[A3 type (KD6R309AX4) (Built-in Illumination Model) Outline]



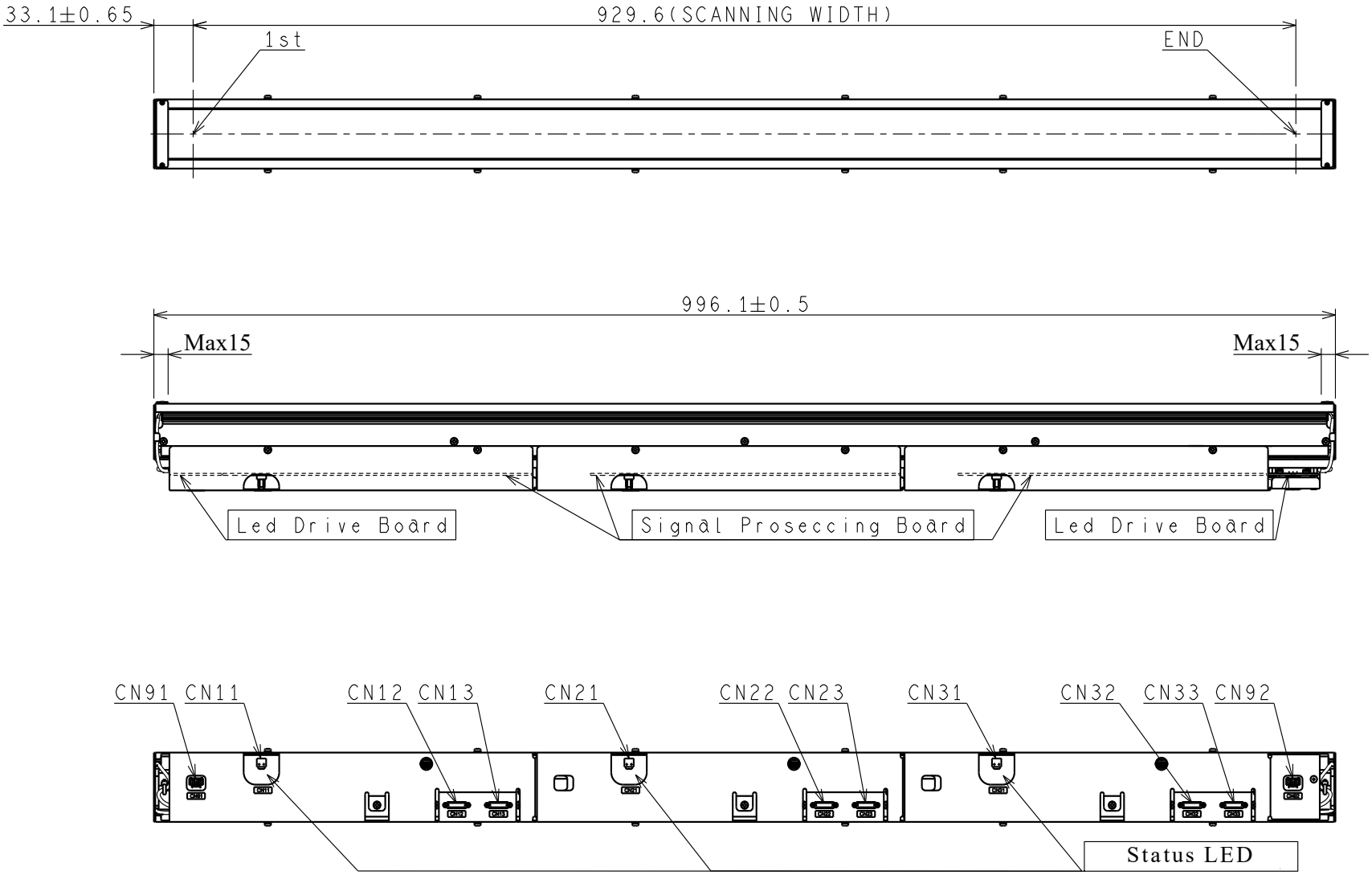
2-7 Specifications

[A1 type (KD6R617AX4) (Built-in Illumination Model) Outline]



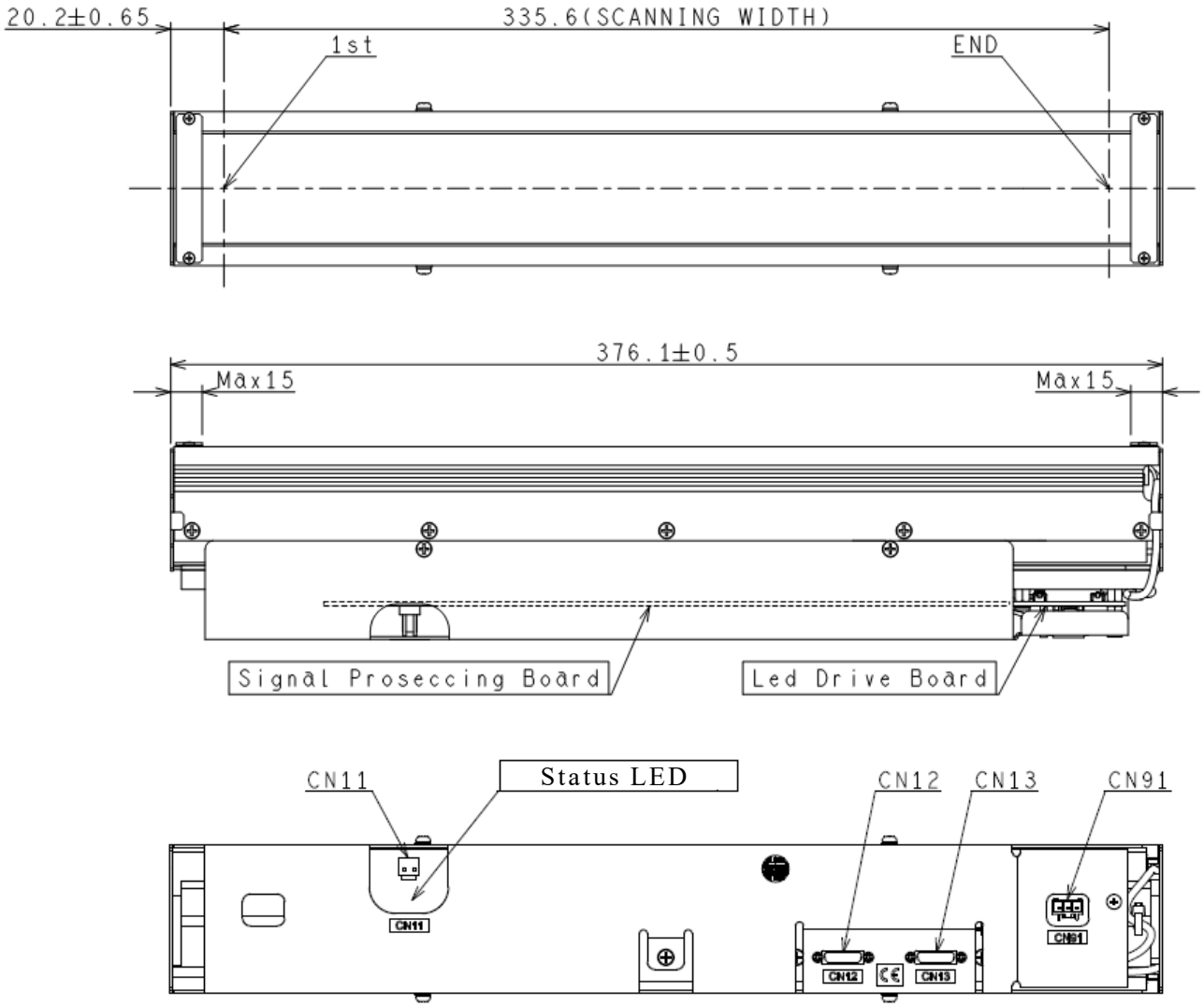
2-7 Specifications

[A0 type (KD6R926AX4) (Built-in Illumination Model) Outline]



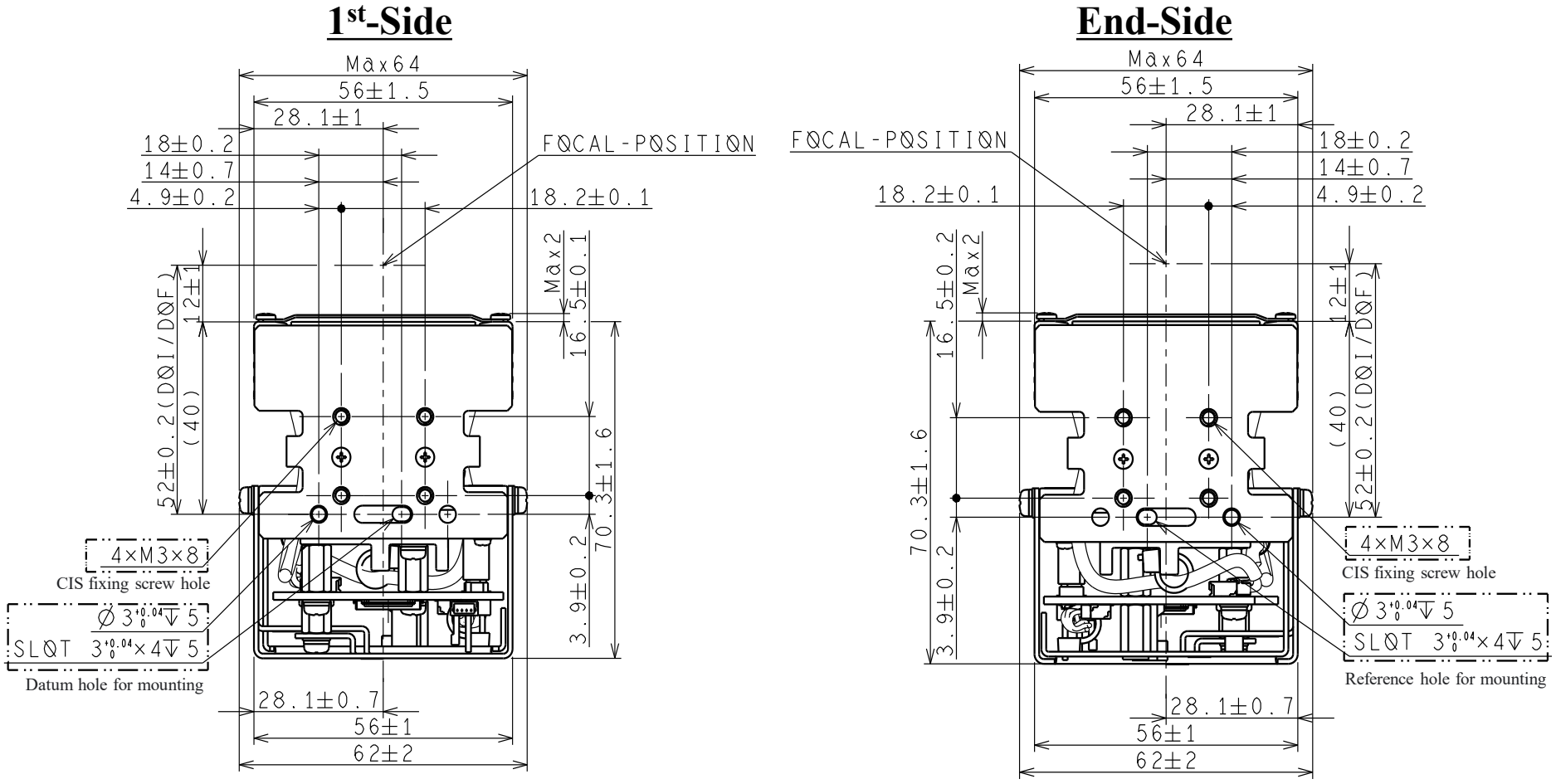
2-7 Specifications

[A3+ type (KD6R335AX4) (Built-in Illumination Model) Outline]



2-7 Specifications

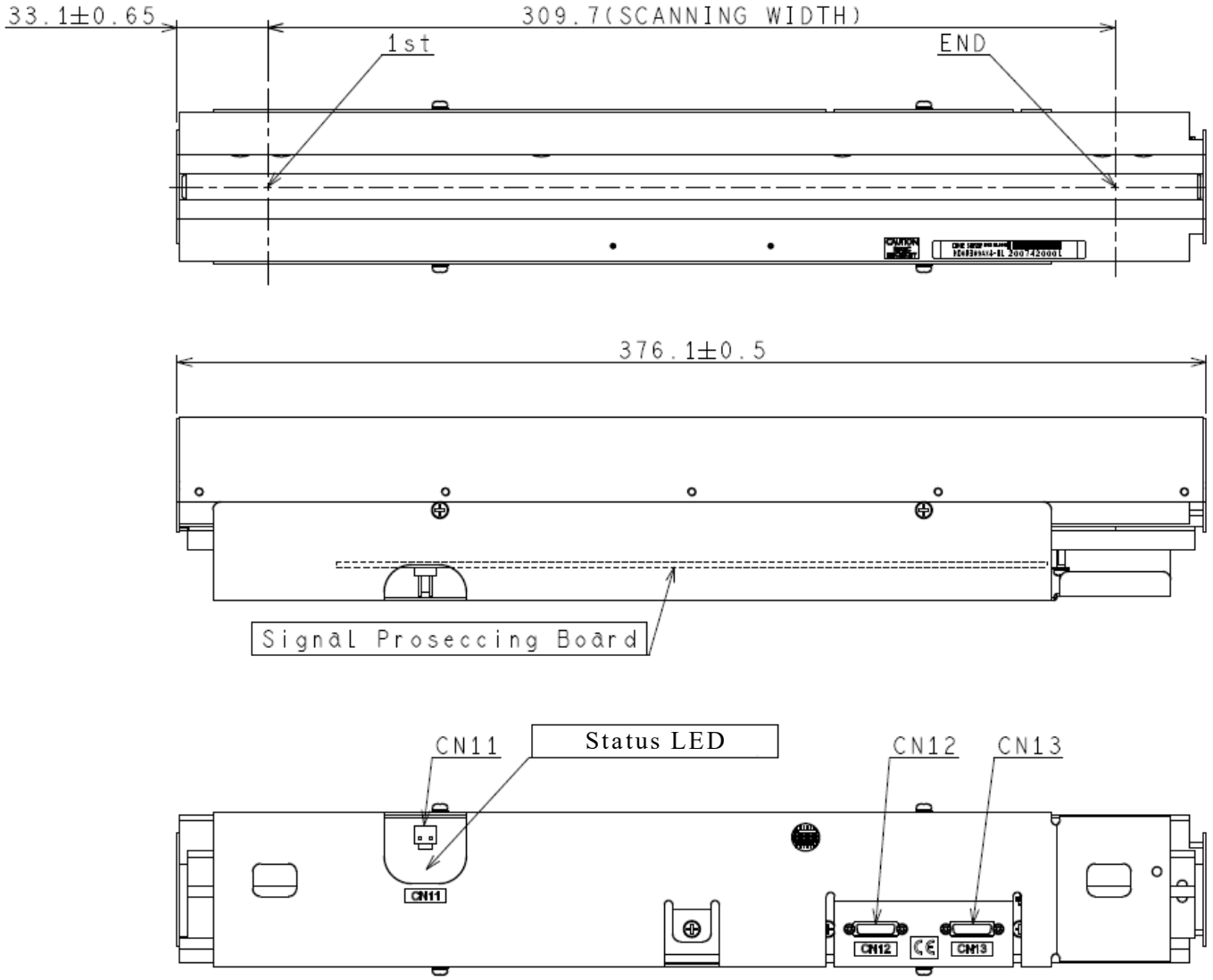
[A3/A1/A0/A3+ type (KD6R309/617/926/335AX4) (Built-in Illumination Model) Common Side View]



CIS should be installed in user's equipment by positioning with a total of 4 mounting datum holes placed on each side of the CIS and fixing the CIS to the user's equipment by using a total of 8 fixing screw holes. (M3 x 4 x 2(both side).)

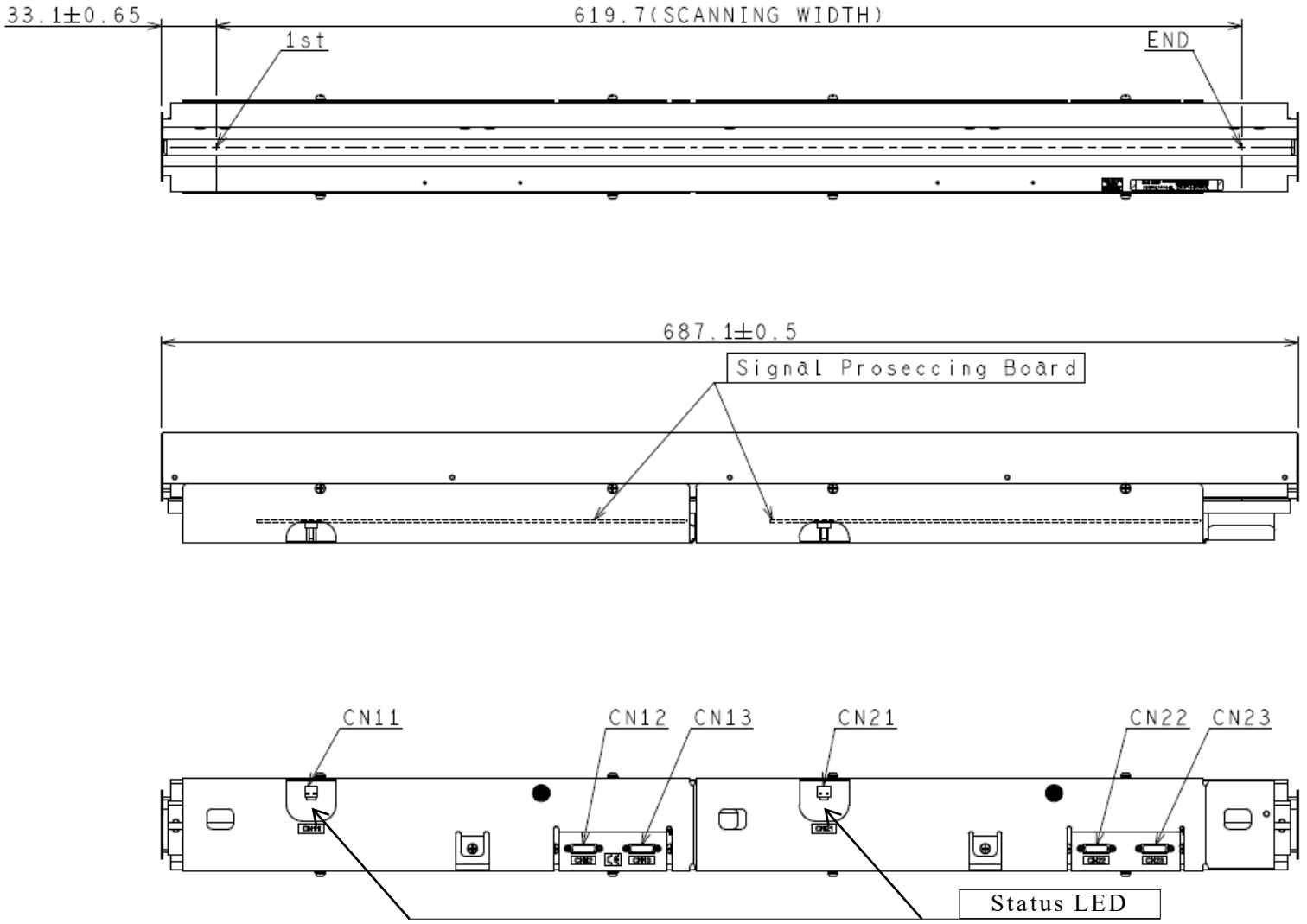
2-7 Specifications

[A3 type (KD6R309AX4-NL) (Non-Illumination Model) Outline]



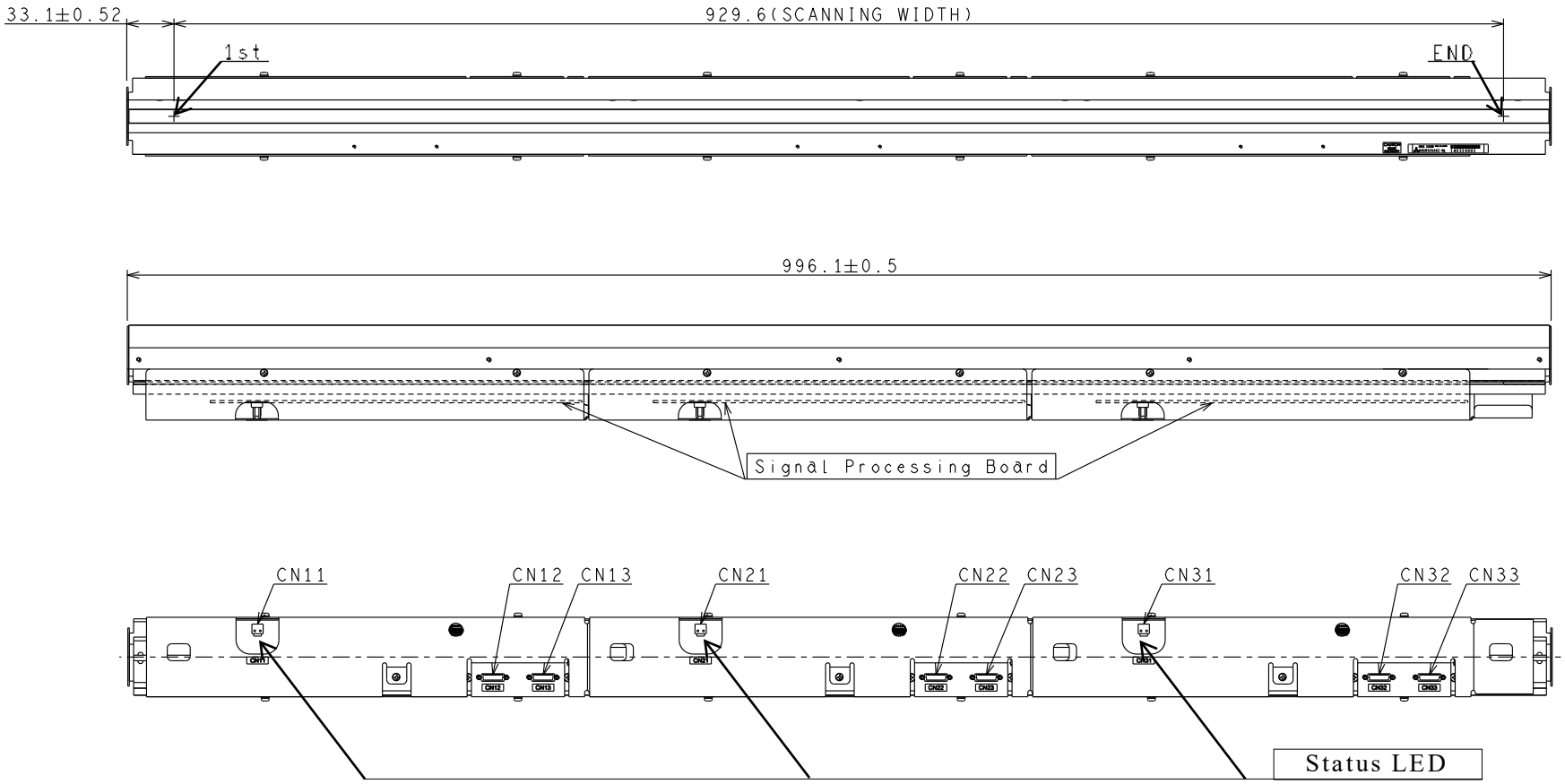
2-7 Specifications

[A1 type (KD6R617AX4-NL) (Non-Illumination Model) Outline]



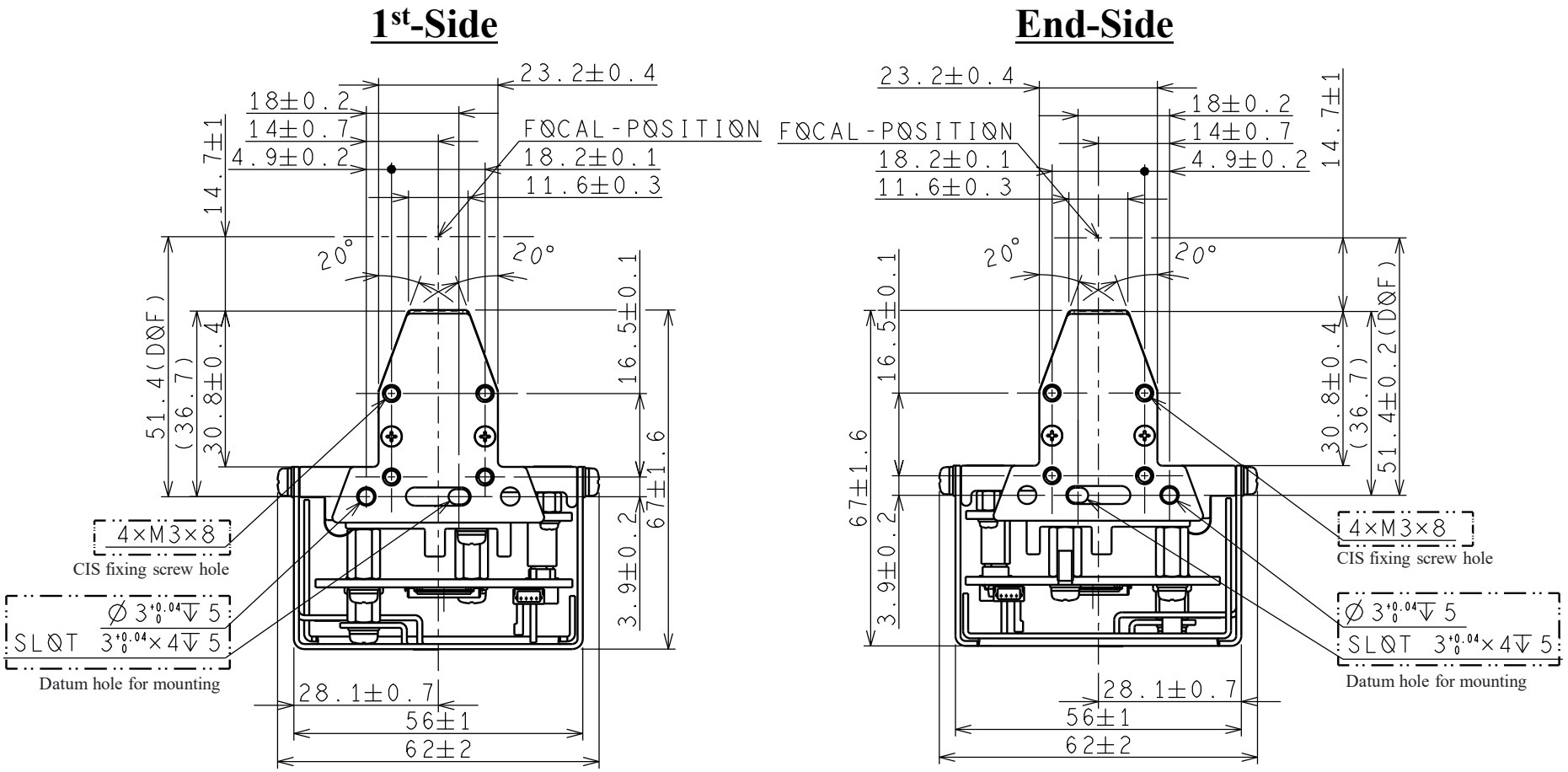
2-7 Specifications

[A0 type (KD6R926AX4-NL) (Non-Illumination Model) Outline]



2-7 Specifications

[A3/A1/A0 type (KD6R309/617/926AX4-NL) (Non-Illumination Model) Common Side View]

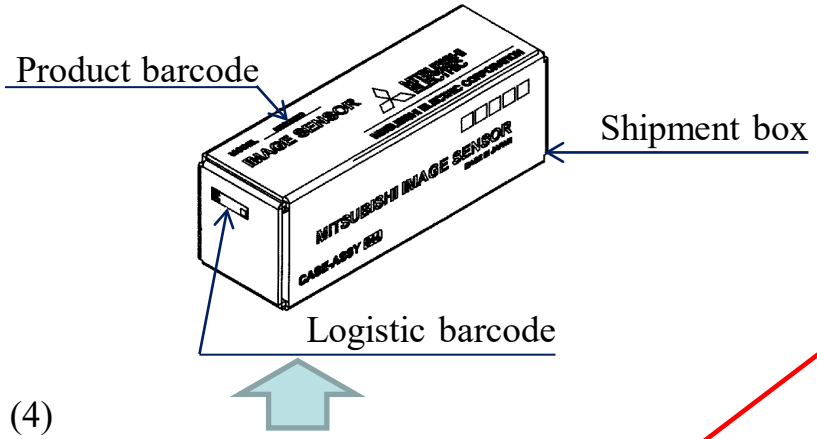


CIS should be installed in user's equipment by positioning with a total of 4 mounting datum holes placed on each side of the CIS and fixing the CIS to the user's equipment by using a total of 8 fixing screw holes. (M3 x 4 x 2(both side).)

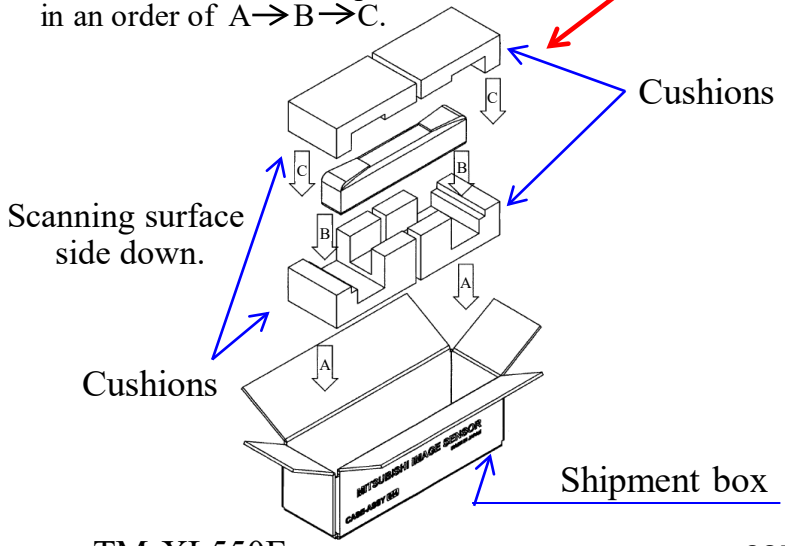
2-7 Specifications (Packaging)

[A3/A1/A0/A3+] （KD6R309/ 617/ 926/ 335AX4）Common Packaging
（KD6R309/ 617/ 926AX4-NL）Common Packaging

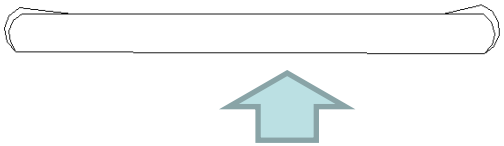
<Shipment box>



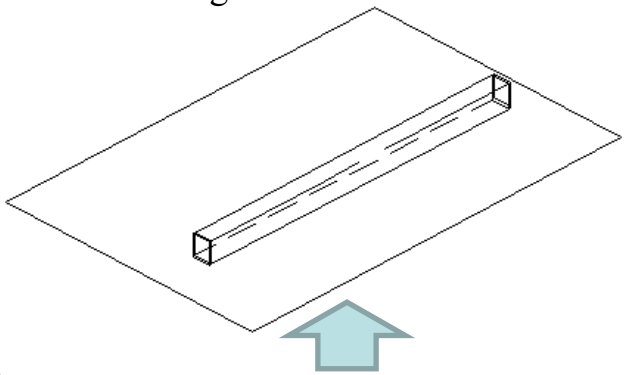
(4)
Pack CIS（2）wrapped by an anti-static sheet and cushions into the shipment box in an order of A→B→C.



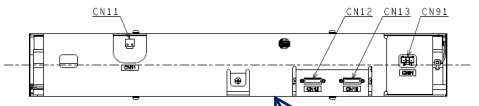
(3) CIS is wrapped with anti-static sheet.



(2) Wrap with anti-static sheet with Scanning surface side down.



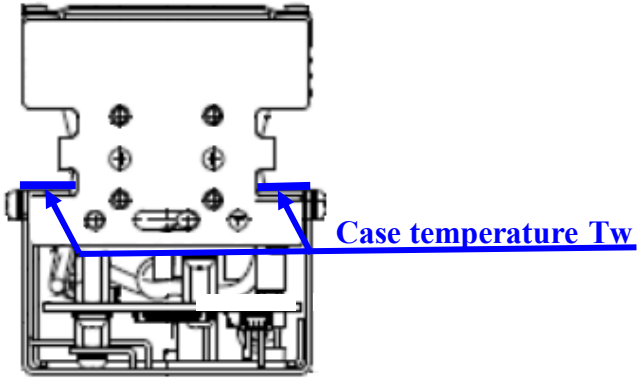
(1)



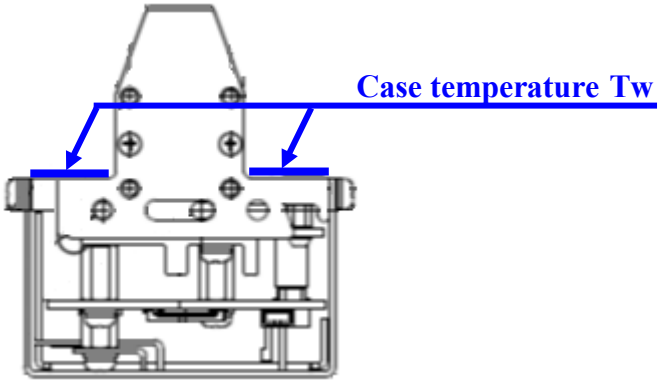
2-8 Handling precautions

<Thermal management>

（Built-in Illumination Model）



（Non-Illumination Model）



(About Thermal management)

This product can be operated under an environmental temperature (Ta) between +5 and +50℃ (in case of L4) under natural air-cooling circumstance.

In other circumstance that the product temperature may be raised by the incoming heat from the peripheral devices and/or the connecting part, check the case temperature Tw (refer left diagram), and control the temperature Tw to be between +5 and +70℃.

If the housing temperature Tw exceeds the temperature range of +5 to + 70 ° C, take forced air cooling or appropriate cooling measures to lower the temperature around the product.

If cooling measures are not taken, it may cause a malfunction or accident.

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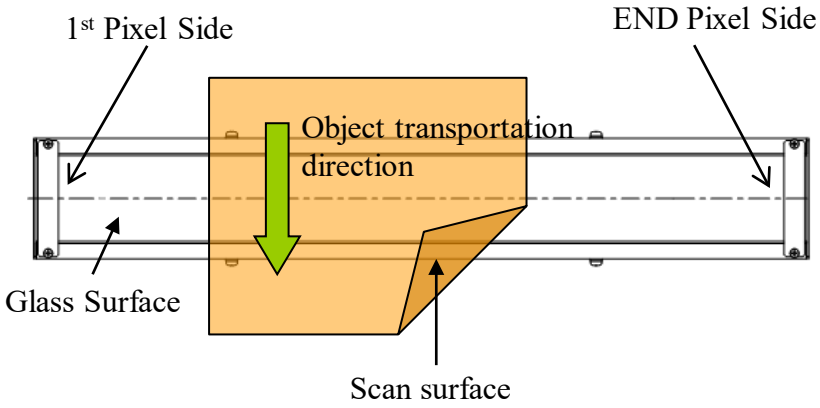
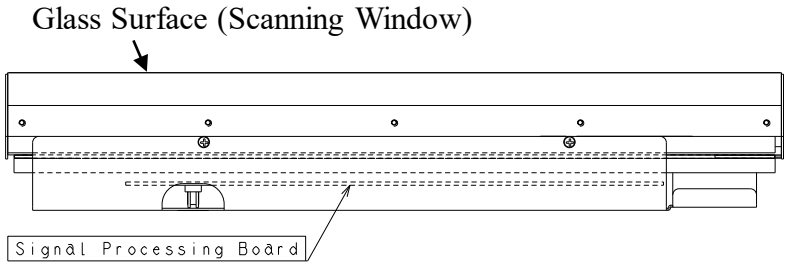
Chapter 3 : Installation

3-1 Installation

3-1-1 Top View



3-1-2 Side View



[Remarks for installation]
Where to place the object and CIS

1. The scanning surface of this product is the glass surface side. Install with the glass surface facing the scanning object.

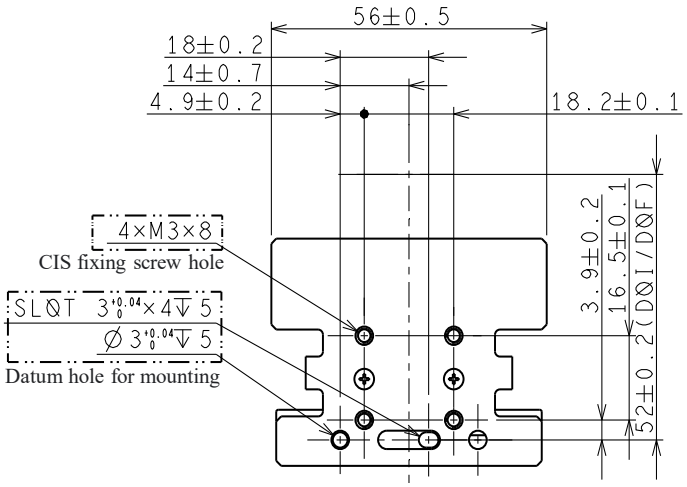
2. Install the upper left side of the scanning surface of the scanning object on the 1st pixel side.

3. An erecting image can be obtained by setting the scanning surface of the scanning object to the CIS side and transporting the object in the direction of the arrow in the figure on the left.

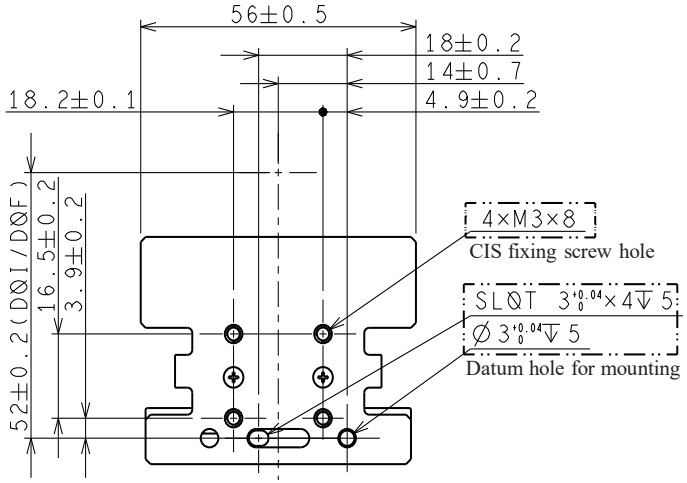
3-1 Installation

3-1-3 Side view of both ends

1st-Side Bracket



End-Side Bracket

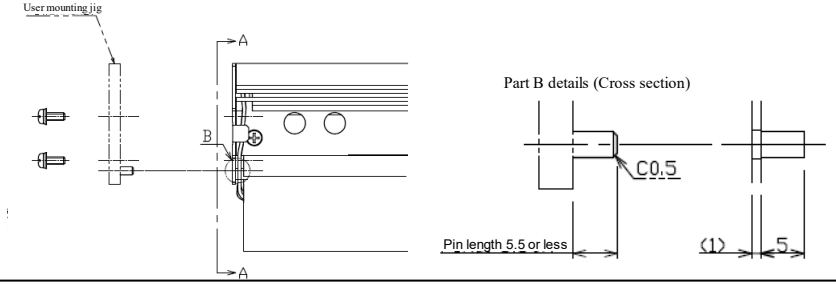


[Remarks for installation]
About the mounting mechanism of CIS

1. Attach to user's equipment on both side of this product.
   The focal position is 52 mm from the Bracket mounting datum hole in the scanning direction.
2. The glass surface is about 12 mm away from the focal position, but its variation depends on the installation orientation and individual product's specification.
3. Fix the CIS to the user's equipment by using the four M3 holes (fixing screw holes) placed on each side of CIS.
   At this time, use the mounting datum holes (Φ3 hole and 3 × 4 long hole) of this product to set the focal position to the correct position in This Product.
4. Make sure to use all 8 fixing points to support the weight of the CIS. The recommended fixing torque is shown in the table below.
5. The Frame material is aluminum. Be careful not to damage the threads when tightening.

Material of screw	Fastening torque [N・cm]
Iron (strength ranking 4.6)	72 ± 7
Stainless (SUS 304)	63 ± 6
Brass (C3601BD)	42 ± 4

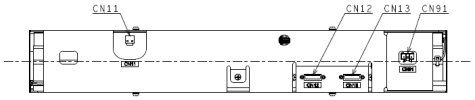
6. The pin length for the datum hole should be 5.5 mm or less.



3-1 Installation

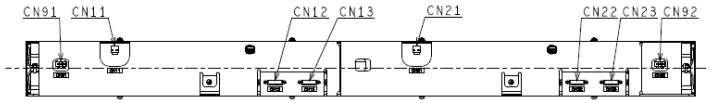
3-1-4 Bottom View

A3（KD6R309AX4/AX4-NL）
A3+（KD6R335AX4）



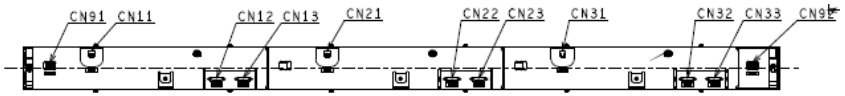
Master Port
CN12

A1（KD6R617AX4/AX4-NL）



Master Port
CN12

A0（KD6R926AX4/AX4-NL）



Master Port
CN22

[Connectors of Interface and Power]

1. The connector for the interface is placed in the bottom of CIS.
2. The connector number is written on the cover in 2-digit as CNxx.
   Left side A3(0～300mm) : CN11, CN12, CN13
   Next side A3(300～600mm) : CN21, CN22, CN23
   Right side A3（600～900mm） : CN31, CN32, CN33
   Connector of Illumination : CN91, CN92
3. Please refer to the table below for each connector type.

Connector type	Connector No.	CIS Model		
		A3 A3+	A1	A0
Power supply for CIS (+5V)	CN11	○	○	○
	CN21	×	○	○
	CN31	×	×	○
Camera Link™ Cable connector *◎: Master Port	CN12	◎	◎	○
	CN13	○	○	○
	CN22	×	○	◎
	CN23	×	○	○
	CN32	×	×	○
	CN33	×	×	○
Power supply for Illuminations（+24V） * Not for Non-Illumination Models	CN91	○	○	○
	CN92	×	○	○

3-2 Preparation

3-2-1 Preparation

*Non-Illumination Model(-NL Series) doesn't need 24V DC cable and 24V power supply.

(1) 5V DC power supply cable (For CIS Sensor drive)

(2) 24V DC power supply cable (For CIS illumination)

(3) Camera Link™ cable
***CIS side is mini Camera Link™.**

(4) DC5V,DC24V Power supply
(5) PC with frame grabber board

Caution: For 5V and 24V cables, consider wiring resistance and prepare as thick a cable as possible. The values in ( ) are reference values.
5V cable standard AWG #16(14Ω/Km)～#22(55Ω/Km)
24V cable standard AWG #20(35Ω/Km)～#22(55Ω/Km)

Please prepare the following items before using CIS.
1. 5V DC Power supply(MAX 3A in A3 units), and the cables.
2. 24V DC Power supply(MAX 3A), and the cables.
3. Camera Link™ cables
   *This Product has the mini Camera Link™ connectors.
4. PC with frame grabber board or image processing board.

No	Item	Quantity		
		A3 A3+	A1	A0
1	5V DC Power supply cable	1	2	3
2	24V DC Power supply cable	1	2	2
3	Camera Link™ cable *At Base Configuration 1, the quantity in ( )	2 (1)	4 (2)	6 (3)
4	5V, 24V DC Power supply	1		
5	PC with frame grabber board	1		

(Notice)
(1) The cables, frame grabber board and power supply are not included with this product
(2) The maximum required value for each current capacity is as follows.

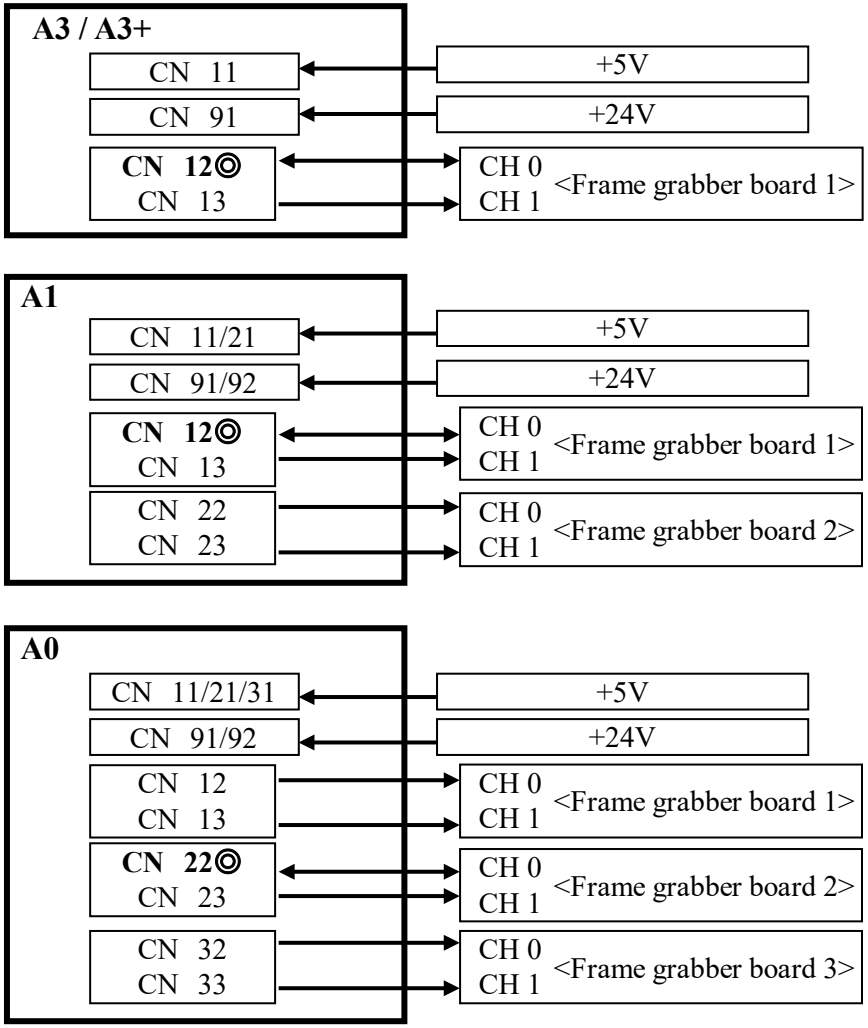
No	Items	Current capacity (A)		
		A3 A3+	A1	A0
1	5V DC Power supply	3	6	9
2	24V DC Power supply	0.8	1.6	2.4

3-3 Connections

3-3-1 Cable connections

* ◎:Master Port

Non-Illumination Model (-NL Series) doesn't have C91 , C92 connector.



[Precautions for connection]

When using multiple Frame Grabber boards, external sync signal input and communication control are possible only from the master port. Please be careful when setting the Frame Grabber board.

(Notice)

(1) This Product is scanning-synchronized in line units. In addition, each A3 unit module also operates with a common CLK signal.

However, there may be deviations due to the distance between the boards and the impedance of the boards, and there is a slight deviation in the CLK signal.

(2) The length of the Camera Link™ cable that connects your control equipment to this product depends on the environment and the state of connection between the equipment. It is the customer's responsibility to select the cable to be used so that communication and image acquisition can be performed normally.

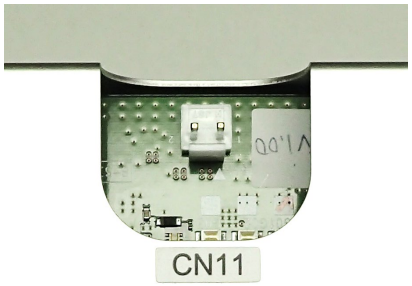
If communication or image acquisition isn't normal, first, lower the camera link frequency (check to the lowest value) and match the cable length recommended by the manufacturer described on page 51 of this document.

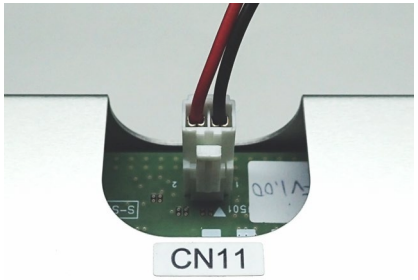
After that, communicate and acquire the image again.

If the camera link™ frequency is lowered and communication and image acquisition are possible according to the cable length recommended by the manufacturer described on page 51 of this document, it isn't a problem of this product itself, but with the customer's control equipment. Please note that we can't compensate.

3-3 Connections

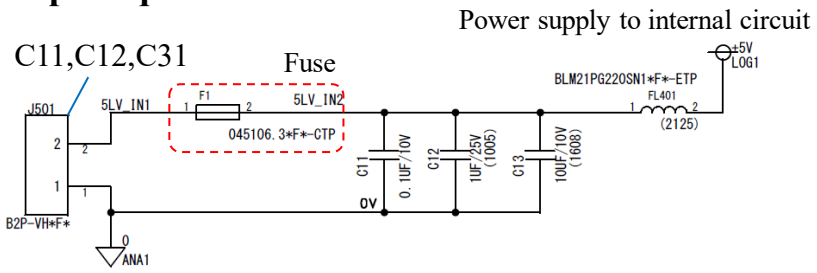
3-3-2 5V DC power supply cable connection





Item	No.	Models		
		A3 A3+	A1	A0
Power supply for CIS (+5V)	CN11	○	○	○
	CN21	×	○	○
	CN31	×	×	○

Input equivalent circuit:



[5V DC power supply cable (For CIS Sensor drive)]

(The cables aren't included with this product)

1. Connect 5V DC power supplies to CN11, CN21, and CN31.

2. This Product has a connector of B2P-VH (made by JST).

3. The following is recommended for the cable side housing for connecting.
   VHR-2N (made by JST).

4. The fuse 045106.3.MRL (made by LITTLE FUSE) is mounted in the internal circuit of this product after 5V connection.

5. The pinout is shown below.

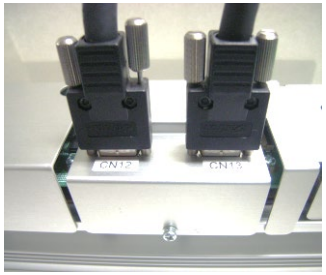
No	Item	Symbol
1	Power supply GND	GND
2	5V DC power supply	VDD

(Caution)
When manufacturing the cable, consider the wiring resistance of the cable and deciding the thickness of the cable. The recommended cable standards for this connector are as follows.
AWG #16 - #22
(This Product recommend using AWG # 16 to minimize power supply voltage drops.)

3-3 Connections

3-3-3 Camera Link™ cable connection

*This Product has the mini Camera Link™ connectors.



Item	No.	Models		
		A3 A3+	A1	A0
Camera Link™ cable *◎ : connect to the master port	CN12	◎	◎	○
	CN13	○	○	○
	CN22	×	○	◎
	CN23	×	○	○
	CN32	×	×	○
	CN33	×	×	○

External sync signal input and communication control of this product are possible only through the master port (common to all sizes).

[Camera Link™ cable]

(The cables aren't included with this product)

1. Connect the Camera Link ™ cable to CN12, CN22, CN32, CN13, CN23, CN33.

2. In Base Configuration 1, Camera Link ™ cable are required 1 for A3, 2 for A1, 3 for A0 and 1 for A3+.
   In Medium Configuration and Base Configuration 2, Camera Link ™ cable are required 2 for A3, 4 for A1, 6 for A0, and 2 for A3+.

3. This product side connector is mounted with 12226-1100-00PL (made by 3M).

4. Use the recommended Camera Link ™ compliant cable below.
   CL-S-SS-020 **(made by Oki Electric Cable Co., Ltd.)**
   DTCL-26P02CC **(made by Daitron Co., Ltd.)**
   In addition, please refer to the notice (2) on the cable connection on page 49, 3-3-1, and select the Camera Link ™ cable.

5. The pinout is Camera Link ™ compliant.

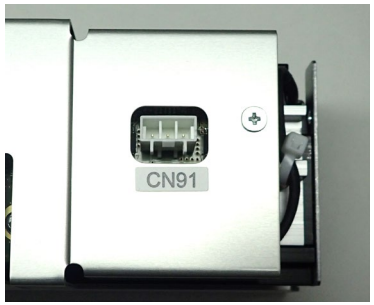
6. The figure on the left shows the location of the master port connector for each product.
   The master port connector number differs depend on the product.
   ・A3, A3+, A1 : CN12
   ・A0 : CN22

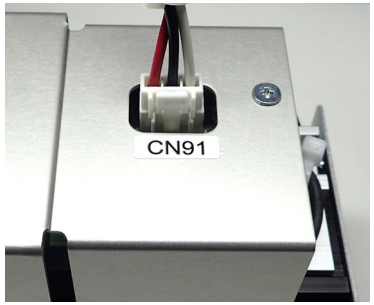
7. The recommended fixing torque is less than 12 N cm.
   If tightened with more torque, the nut on the product side may loosen when the cable is removed.

3-3 Connections

3-3-4 24V DC power supply cable connection

*Non-Illumination Model(-NL Series) doesn't need 24V DC cable.

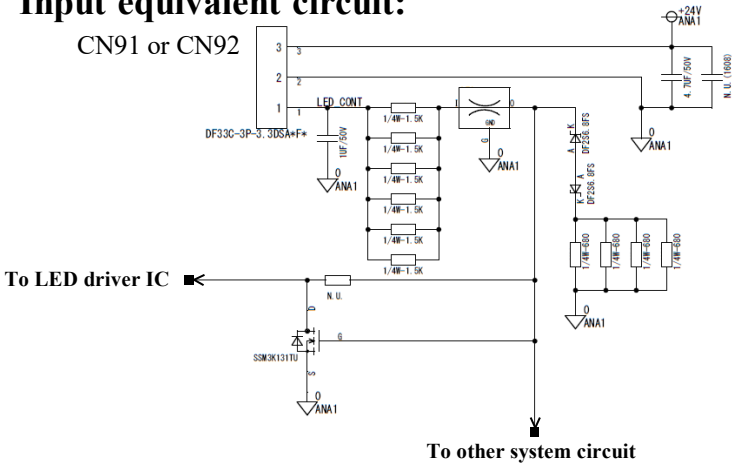




Item	No.	Models		
		A3 A3+	A1	A0
Power supply for Illuminations (+24V)	CN91	○	○	○
	CN92	×	○	○

Input equivalent circuit:

CN91 or CN92



[24V DC power supply cable (For CIS illumination)]

(The cables aren't included with This Product)

1. Connect 24V DC power supplies to CN91 and CN92.
2. This product has a connector of DF33C-3P-3.3DSA (made by HIROSE). The following is recommended for the cable side housing for connecting. DF33C-3S-3.3C(made by HIROSE).
3. Registers can be set by serial communication of Camera Link™.
4. By using the 1-pin control signal port, you can directly control the LED lighting ON / OFF by an external signal. Control with an open collector circuit. If the voltage isn't low enough, the illuminations may not turn on. * illuminations On / Off and illuminance can be controlled by register with serial communication on Camera Link™.
5. If you do not directly control the LED lighting, connect pin 1 to GND with low impedance.
6. For the 24V power supply, it is recommended to control ON / OFF while the 5V power supply is ON. However, even if the timing of 5V and 24V is reversed, it will not fail. For details, refer to Chapter 4, Startup Sequence.

* Cable standard: AWG # 20 to # 22 (# 20 is recommended to suppress the influence of power supply voltage drop)

No	Item	Symbol	I/O	Signal
1	LED illumination Control Line	CONT	I	OPEN : Turn OFF GND : Turn ON
2	GND	GND-LED	—	GND for Illuminations
3	+24V Power supply	VLEDI	—	24V power supply for Illuminations

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Chapter 4 : How to control CIS

*** In this document, all numerical values with "h" or "0x" after this page are equally "hexadecimal".**
Basically, "0x" notation is used for register addresses and commands, and "h" notation is used for register setting values alone.
Also, all values with "b" are "binary".
Numbers without anything at the end are "decimal".

4-1 Startup procedure

Turn on the power of CIS and LED illuminations.

- Turn on the 5V power supply for CIS and the 24V power supply for LED illuminations (in the case of built-in illuminations).
  * It is recommended to turn on the power at the same time or turn on the 5V power supply first.。
  Before turning on the 5V power, turn on the 24V power and do not leave it for a long time. It may cause malfunction or damage.
- Before turning on the power of CIS, it is recommended to start up the communication / control device (PC, etc.) with CIS in advance.
  (This is because you need to prevent CIS communication errors due to indefinite state input from the control device.)

Confirm that the CIS boot is complete.

- Status LED will turn to green after boot up.(Lights orange during boot)
- Regardless of whether the mode is external sync or internal sync, the Status LED will immediately switch to blinking green if a sync signal is being input.

*When you continue to input the sync signal, you can't see the green lighting and it will change to green blinking.

Serial Communication (UART) Settings via Camera Link™.

- Settings of this product can be controlled by Serial Communication (UART) via SERTC/SERTFG pin on the Camera Link™.
- Baud rate (initial setting) is 19.2kbps.

Control CIS by frame grabber control software. (Refer to Chapter 5 for details on control functions.)

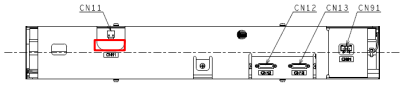
- The picture data can be taken by software which is attached with grabber board.

* Refer to <Appendix A-3: Register list> on a list of register addresses for function settings.

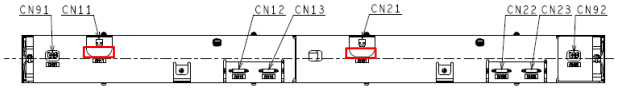
4-2 LED indicator

4-2-1 LED indicator

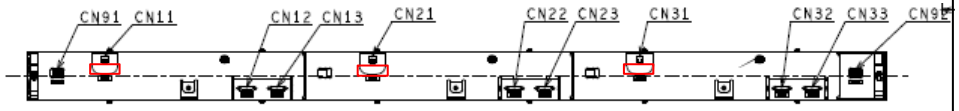
A3(KD6R309AX4/AX4-NL)、A3+(KD6R335AX4)



A1(KD6R617AX4/ AX4-NL)



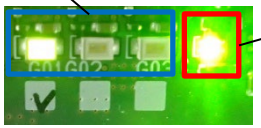
A0(KD6R926AX4/ AX4-NL)



LED Status	CIS Status
LED Off	No Power
Orange LED On	During system boot
Green LED On	Boot complete, no stream transfer
Green LED Blinking 0.5 sec	Boot complete, transferring stream

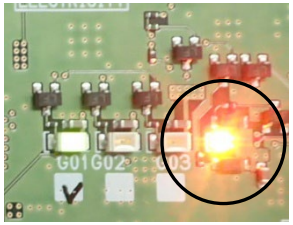
1. Arrangement of Status LED

Ignore the 3 LEDs on the left
（LED for product management）

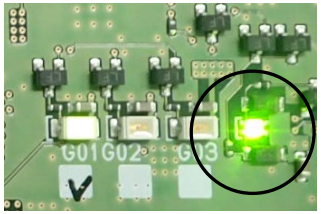


2. Example of lighting the Status LED

LED Status
Orange LED On



LED Status
Green LED On



(Notice) Do not enter commands or enter signals in the indefinite state of the user control device until the system boot is completed, the sync signal is input, and the flashing green state is displayed.

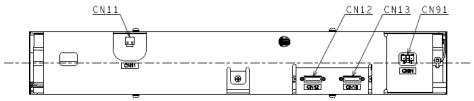
If you input the signal during the above period, an error will occur and the command may not be accepted until the serial communication timeout function is enabled (initial value: about 0.2 seconds).

When a timeout occurs, "0x11" is answered and the communication status is reset and communication is restored.

4-3 Master and Slave Port for Communications

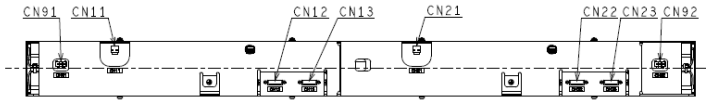
4-3-1 Master and Slave Port of Communication

A3（KD6R309AX4/AX4-NL）、A3+（KD6R335AX4）



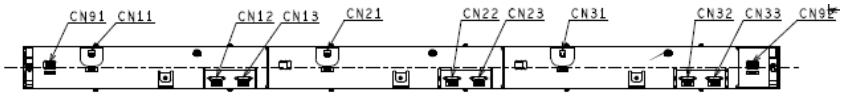
Master Port
CN12

A1（KD6R617AX4/AX4-NL）



Master Port
CN12

A0（KD6R926AX4/AX4-NL）



Master Port
CN22

[Control Method]

Regardless of the size of this product, sync signal input and communication control are possible only from the master port built into the Camera Link ™ I / F.

Ports other than the master port are called slave ports.

[Control from Master Port]

- External sync signal input（CC1）
- Serial Communication（UART）

[Master Port Connector]

The figure on the left shows the location of the master port of the Camera Link ™ I / F for which communication of each product is valid. The master port connector number differs depending on the product.

- A3, A3+, A1 : CN12
- A0 : CN22

[Notice]

(1) CIS can be controlled only through Master port.
(Signal through the other ports will not be reflected to CIS.)

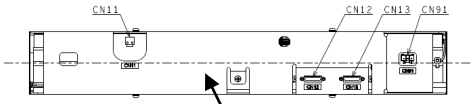
(2) In advance, confirm where to be connected from your Grabber board.

(3) The initial value of the communication speed (Baud rate) is 19.2 kbps, and you can select 9.6 kbps, 19.2 kbps, or 115.2 kbps by changing the setting.
Please note that communication will not be possible if the Baud rate setting of this product and the Baud rate of the prepared communication software are different.

4-3 Master and Slave Port for Communications

4-3-2 Communication destination for each size

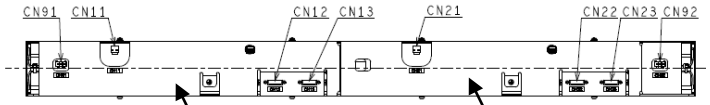
A3（KD6R309AX4/AX4-NL）, A3+（KD6R335AX4）



First Pixel Side　　End Pixel Side

FPGA1
ASIC1
ASIC2

A1（KD6R617AX4/AX4-NL）

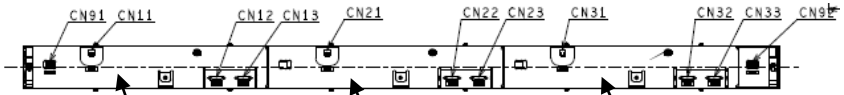


First Pixel Side　　End Pixel Side

FPGA1	FPGA2
ASIC1	ASIC3
ASIC2	ASIC4

A0（KD6R926AX4/AX4-NL）

First Pixel Side　　End Pixel Side



FPGA3	FPGA1	FPGA2
ASIC5	ASIC1	ASIC3
ASIC6	ASIC2	ASIC4

[Communication for each size]

The communication destination of this product is as shown on the left.

Specify the communication destination by UART communication from the master port.

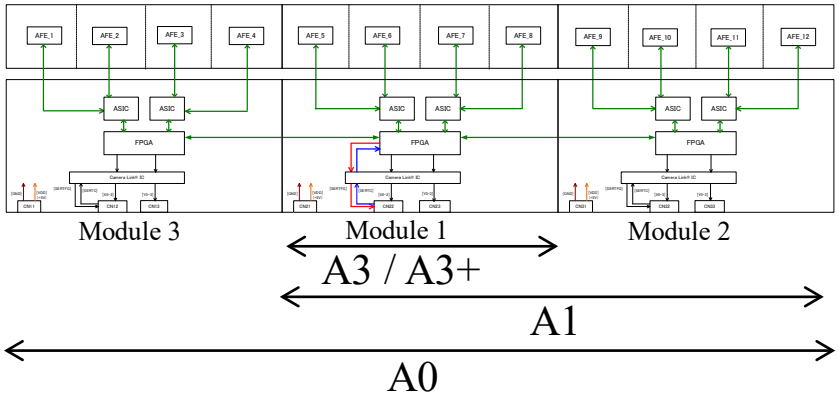
Refer to P.60 4-4-3 Command List for a list of commands for specifying a communication destination.

Depending on the size, some devices may not have a communication destination, so you cannot specify a device without specifying the communication destination.

①Case for A3 or A3+ size.
There are no Setting Device of FPGA2～3 and ASIC3～6.
②Case for A1 size.
There are no Setting Device of FPGA3 and ASIC6.

4-4 Communication control (overview)

4-4-1 Communication control block diagram



Red line / blue line: Serial communication (UART)
Green line : SPI communication (internal only)

・Select the communication Baud Rate

You can change the Baud Rate by registers setting with the Camera Link ™ UART.
Please note that communication will only be accepted at the changed Baud Rate.
Baud Rate does not depend on EEPROM boot and always sets at 19.2kbps at startup.

For details, refer to P61 4-4-4 Communication setting registers.

[Communication Path]

(1) As shown in the figure on the left, this product can be controlled from the outside using the SERTC / SERTFG terminal of the Camera Link™ specifications. Users can control communication for the following settings.
- FPGA / ASIC Register Read / Write
- FPGA / ASIC Status Register Read / Write
- EEPROM Read/ Write

(2) Communication Specifications

Baud rate	9.6k, 19.2k, 115.2k bps
Data bit	8bit
Parity	None
Stop Bit	1bit
Flow Control	None
Bit Order for Transmission	LSB(Least Significant Bit) First

1. The initial setting of Baud Rate is 19.2kbps. Use the same Baud Rate for all modules.
2. This product internally performs serial communication (UART) → SPI conversion and is controlled by SPI communication.
3. The DIP switch on the board is placed in the back of the cover so that the settings cannot be changed, please don' t touch it. Please note that we must not be responsible for any malfunction of This Product caused by changing the DIP switch.

4-4 Communication control (overview)

4-4-2 Command Format and Command Example

(1) Status register Write Example: Select the SRAM area for Dark correction of ASIC1

0x1B 0x14 0x00 0x02 0x01 0x04 0xFF

No.1 2 3 4 6 7

(2) Status register Read Example: Check the status of FPGA1

0x1B 0x73 0x00 0x02 0x05 0xFF (0x00/0x01)

No.1 2 3 4 7 6 (Returned value)

(3) Register Write Example: Write 3 bytes of data from ASIC1 address 0x1CFC

0x1B 0x12 0x00 0x06 0x02 0x1C 0xFC 0x00 0x01 0x03 0xFF

No.1 2 3 4 5 6 7

(4) Register Read Example: Read 3 bytes of data from ASIC1 address 0x1CFC

0x1B 0x12 0x00 0x06 0x03 0x1C 0xFC 0xFF (0x00 0x01 0x03)

No.1 2 3 4 5 7 6 (Returned value)

[Explanation table for each item]

No.	Item	Size (Byte)	Explanation
1	Start Code	1	Fixed to 0x1B. Command start code.
2	Command	1	Read / Write destination, and select Read / Write control mode.
3	Parameter Size	2	Total number of bytes of Instruction Code , Address and Parameter Data.
4	Instruction Code	1	Select SPI control operation mode.
5	Address	2	Specifies the Read / Write register or memory address.
6	Parameter Data	1～255	Register data, Memory data
7	End Code	1	Fixed to 0xFF. Command exit code.

Instruction Code	Description
0000 0011 (0x03)	Read Data
0000 0010 (0x02)	Write Data
0000 0101 (0x05)	Read Status Register
0000 0001 (0x01)	Write Status Register

[Command set]

This Product can be controlled by serial communication (UART). The format of the command used for serial communication is shown in the figure on the left. Please refer to the “explanation table for each item” for each function.

[Notice]

(1) In the command, set the communication destination and Read / Write. This Product is equipped with multiple ASICs and FPGAs. When communicating, check the communication destination in the block diagram and the command list on the next page. In the general use, CIS can be controlled by setting to ALL ASIC (0xA2) and ALL FPGA (0xB2).

(2) For the detailed procedure of CIS internal setting, refer to Chapter 5 and the Functional Specifications.

(3) **It is possible to read and write to the built-in EEPROM, but it is the user's responsibility to switch the internal signal before performing.**
Refer to the Function Specifications (TM-XL551) and fully understand before rewriting or setting the built-in EEPROM.
We recommend that you make a backup of the settings in the EEPROM so that you can restore them if you make a mistake.

(4) When the communication with the EEPROM is finished, be sure to return the Status Register bit 0 of the Master FPGA to "0" to prevent typographical errors. If you write without returning, the data in the EEPROM that you didn’t intend will be rewritten.

(5) During the startup of this product, if a wrong command is sent or a wrong signal is input due to an indefinite state of the control device on the user, communication may be fixed and communication may not be possible. FPGA register address 0x0116 (communication) will be automatically reset at the set time (timeout setting register).
(Refer to the communication setting register section on P61 4-4-4.)
However, in order to start communication stably, we recommend turning on the power of CIS after completing the startup of user’s communication / control device (PC, etc.).

4-4 Communication control (Communication destination)

4-4-3 Command List

※When ASIC and FPGA aren't individually controlled, only the commands surrounded by the red can control communication.

Command	Communication destination / Function	Size of CIS	Command	Communication destination / Function	Size of CIS
0x11	ASIC1 Register Read	309/617/926/335	**0x62**	ASIC6 Register Write	926
0x12	ASIC1 Register Write		**0x63**	ASIC6 Status Register Read	
0x13	ASIC1 Status Register Read		**0x64**	ASIC6 Status Register Write	
0x14	ASIC1 Status Register Write		**0x71**	FPGA1 Register Read	309/617/926/335
0x21	ASIC2 Register Read		**0x72**	FPGA1 Register Write	
0x22	ASIC2 Register Write		**0x73**	FPGA1 Status Register Read	
0x23	ASIC2 Status Register Read		**0x74**	FPGA1 Status Register Write	
0x24	ASIC2 Status Register Write		**0x81**	FPGA2 Register Read	617/926
0x31	ASIC3 Register Read	617/926	**0x82**	FPGA2 Register Write	
0x32	ASIC3 Register Write		**0x83**	FPGA2 Status Register Read	
0x33	ASIC3 Status Register Read		**0x84**	FPGA2 Status Register Write	
0x34	ASIC3 Status Register Write		**0x91**	FPGA3 Register Read	926
0x41	ASIC4 Register Read		**0x92**	FPGA3 Register Write	
0x42	ASIC4 Register Write		**0x93**	FPGA3 Status Register Read	
0x43	ASIC4 Status Register Read		**0x94**	FPGA3 Status Register Write	
0x44	ASIC4 Status Register Write		**0xA2**	ALL ASIC (ASIC1～6) Register Write	309/617/926/335
0x51	ASIC5 Register Read	926	**0xA4**	ALL ASIC (ASIC1～6) Status Register Write	
0x52	ASIC5 Register Write		**0xB2**	ALL FPGA (FPGA1～3)Register Write	
0x53	ASIC5 Status Register Read		**0xB4**	ALL FPGA (FPGA1～3) Status Register Write	
0x54	ASIC5 Status Register Write		**0xC3**	Master FPGA (FPGA1) Status Register Read	
0x61	ASIC6 Register Read		**0xC4**	Master FPGA (FPGA1) Status Register Write	

4-4 Communication control (communication setting register)

4-4-4 Communication setting register

[Settings]
Command setting destination : FPGA (Example :0xB2 ALL FPGA)

Address	Register Name	Function
0x4001	BAUD_RATE	Select Baud Rate **"0" (00h) 9.6kbps** **"1" (01h) 19.2kbps** **"2" (02h) 115.2kpbs** **"3" (03h) 19.2kbps**
0x0116	TIMEOUT	Communication reset ON / OFF and time set **"0" (00h) Invalid** - (No reset when communication error occurs) **"1" (01h) valid** - In case of communication error, This Product will reset in 0.2 sec. **"2"～"255" (02h～FFh) Valid** - The time until the reset is extended by the set value ((decimal number) x 0.2 sec). **(Return value when communication reset)** **When the communication reset, 0x11 is output as a return value from This Product.** Communication is possible again immediately after receiving the return value. There is no return value from This Product other than communication reset.

[Register maps]

	b7	b6	b5	b4	b3	b2	b1	b0
0x4001							BAUD_ RATE(1:0)	
0x0116	TIMEOUT(7:0)							

[Communication settings via UART]

[Function]
Set the baud rate via the Camera Link ™ UART.
In addition, set the ON / OFF of the function that resets in a certain period when a communication error occurs and the period until reset.

[Initial Setting]
Baud Rate 19.2kbps **(0x4001 = 03h)**
Reset setting in case of communication error ON 0.2sec **(0x0116 = 01h)**

[Setting mode]
1. Baud Rate 3types (Compliant with Camera Link™)
2. Set the time until communication reset when a communication error occurs

[Notice]

(1) If the timeout function of register address 0x0116 is disabled by setting to "0" (00h), recover from a communication error by turning the power off and then on again.
(2) If you change the Baud Rate, communication will be accepted only at the changed Baud Rate. Change the settings on the User's control software to the same Baud Rate.
(3) When powered on, the Baud Rate is always set at 19.2kbps.
(4) When a communication reset occurs, "0x11" is answered, the communication status is reset, and communication is restored.

Example of Communication Command

Setting Baud Rate to 9.6kbps
0x1B 0xB2 0x00 0x04 0x02 0x40 0x01 0x00 0xFF
Reset setting in case of communication error is OFF(invalid)
0x1B 0xB2 0x00 0x04 0x02 0x01 0x16 0x00 0xFF

4-4 Communication control (Register control AX3 compatibility mode)

4-4-5 Register control AX3 Compatibility Mode

[Settings]
Command setting destination : FPGA1 (Example :0xB2 ALL FPGA)

Address	Register Name	Function
0x3390	UCOMSEL	Communication mode “0”: AX4 original “1”: AX3 compatibility mode

[Register maps]

	b7	b6	b5	b4	b3	b2	b1	b0
0x3390								UCOM SEL

[Register control AX3 Compatibility mode]
[Function]
Setting the communication mode to AX3 compatibility mode controls FPGA register bit allocation and ASIC register address in an AX3-compatible state It will be possible.
[Initial Setting]
Communication mode AX4original **(0x3390 = 00h)**
[Setting mode]
Communication mode AX4original or AX3 compatibility mode

Example of Communication Command

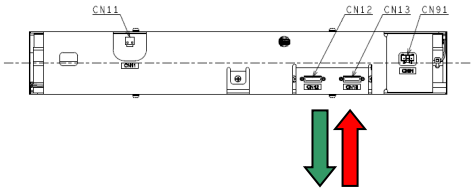
Setting AX4 original
0x1B 0xB2 0x00 0x04 0x02 0x33 0x90 0x00 0xFF
Setting AX3 compatibility mode
0x1B 0xB2 0x00 0x04 0x02 0x33 0x90 0x01 0xFF

[Notice]
Even if AX3 compatibility mode is set, some functions are not compatible, so please check the operation sufficiently before using it after replacing the AX3.
For details of compatibility functions, refer to TM-XM568A.

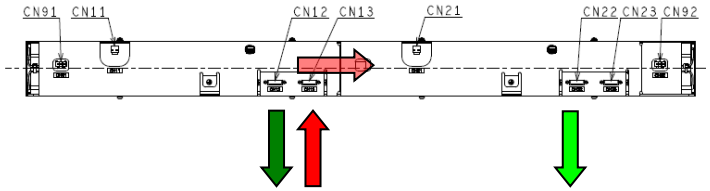
4-5 Line Sync Input

4-5-1 External sync signal input

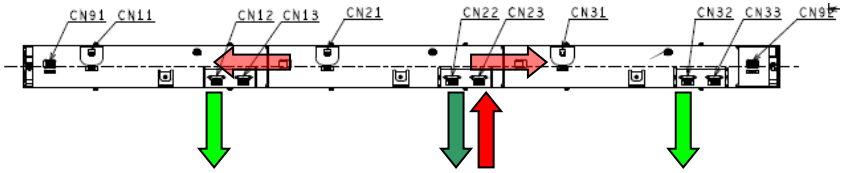
A3（KD6R309AX4/AX4-NL）、A3+（KD6R335AX4）



A1（KD6R617AX4/AX4-NL）



A0（KD6R926AX3/AX3-NL/AX3BK）



Sync signal input, serial communication input.

Image output, serial communication return value output.

Image output.

[Line sync signal]

The external sync signal , input through the camera Link™ I / F Master Port Pin (CC1) , is distributed to other blocks in this product. The line date from each block is synchronized at line scanned basis.

[Internal Sync Mode]

The internal sync signal generated by the A3 board unit module with the Master Port is distributed to other A3 board modules. The line date from each block is synchronized at line scanned basis to all scanned pixels.

[Notice]

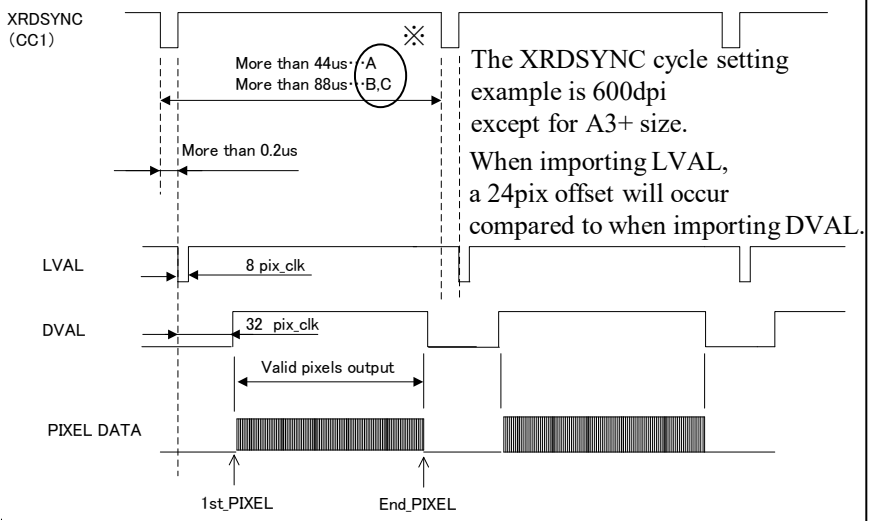
This product consists of modules at the A3 board basis.

Each module is synchronized with the main CLK and read-synchronized on a line basis, there are some cases gap between the boards cause a little gap.

Although, the gap that occurs doesn't affect the image output at all.

4-6 Line Sync Timing（External Sync mode）

4-6-1 Line sync Timing (External Sync)



Sync signal timing chart

※

A 24-bit RGB Color × 2Tap Medium Configuration (@84MHz)
B 24-bit RGB Color Base Configuration (@84MHz)
Based on Camera Link™ specifications
or 24-bit RGB Color Base Configuration × 2 (@84MHz)
Based on Camera Link™ specifications × 2
C 30-bit RGB Color Medium Configuration (@84MHz)
Based on Camera Link™ specifications

Example of Communication Command

Switch from internal sync mode to external sync mode again

0x1B 0xB2 0x00 0x04 0x02 0x01 0xA0 0x01 0xFF

[External Sync Mode]

※This Product is set to the external sync mode by default at the shipment.
※For details of the settings, refer to "P.75 5-2 Setting 4: Line Sync Input".

(1) To operate CIS at the external sync mode, input through the sync signal is necessary.

(2) Input the sync signal (trigger signal corresponding to XRDSYNC in the figure on the left) from the CC1 terminal of the Camera Link™ I / F board from Master Port.

(3) The Image scanning operation is based on the falling edge of XRDSYNC. For stable operation, secure 0.2 µsec or more for the "L" period shown on the left for XRDSYNC.

(4) When the synchronization signal is input to CC1 from the encoder of the subject carrier via each grabber boards and used, The Image scanning speed control according to the transport speed becomes possible.

(5) The offset of the sensor pixel output start position and the setting of the number of effective output pixels can be changed. For details, refer to P.76 "5-2 Setting 5 Output Width Setting".

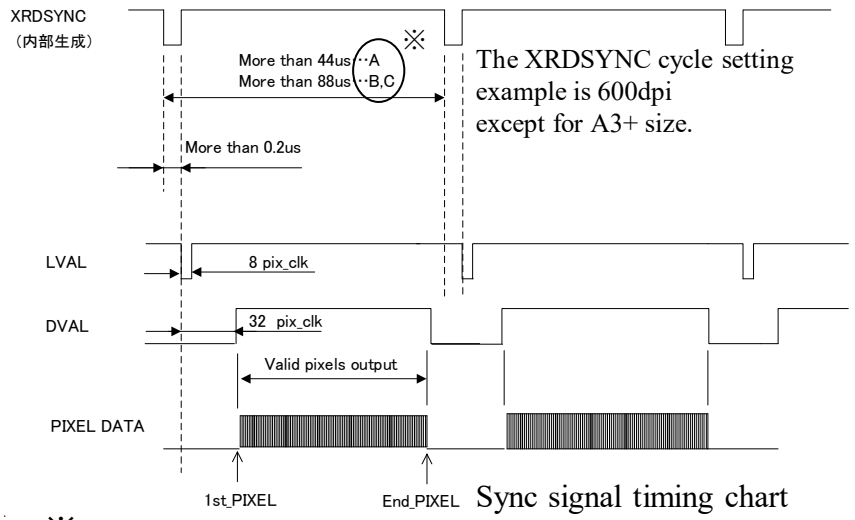
[Notice]

(1) Input/set the longer sync signal cycle than the line cycle. Image data cannot be output normally if the line period is shorter than the required line period.

(2) Don't use images (data) for 10 lines immediately after the sync signal is input. Invalid images and uncorrected images are output.
(Because there is a line delay in the internal signal processing circuit.)

4-6 Line Sync Timing（Internal Sync mode）

4-6-2 Line sync Timing (Internal Sync.)



Sync signal timing chart

※
A 24-bit RGB Color × 2Tap Medium Configuration (@84MHz)
B 24-bit RGB Color Base Configuration (@84MHz)
Based on Camera Link™ specifications
or 24-bit RGB Color Base Configuration × 2 (@84MHz)
Based on Camera Link™ specifications × 2
C 30-bit RGB Color Medium Configuration (@84MHz)
Based on Camera Link™ specifications

Example of Communication Command

When using the internal sync. mode at 44 µsec / Line.

0x1B 0xB2 0x00 0x04 0x02 0x01 0xA2 0x0E 0xFF
0x1B 0xB2 0x00 0x04 0x02 0x01 0xA1 0x6F 0xFF
0x1B 0xB2 0x00 0x04 0x02 0x01 0xA0 0x00 0xFF

When using the internal sync. mode at 88 µsec / Line.

0x1B 0xB2 0x00 0x04 0x02 0x01 0xA2 0x1C 0xFF
0x1B 0xB2 0x00 0x04 0x02 0x01 0xA1 0xDF 0xFF
0x1B 0xB2 0x00 0x04 0x02 0x01 0xA0 0x00 0xFF

[Internal Sync. Mode]

※This Product is set to the external sync. mode by default at the shipment.
※For details of the settings, refer to “P.75 5-2 Setting4: Sync. signal input settings”.

(1) The sync. signal can be generated inside this product.

(2) When using in the internal sync. mode, be sure to set the line cycle before the image scanning operation.

(3) As with external sync. mode, the offset of the sensor pixel output start position and the setting of the number of effective output pixels can be changed. For details of the settings, refer to “P.75 5-2 Setting 4 : Sync. signal input settings”.

[Notice]

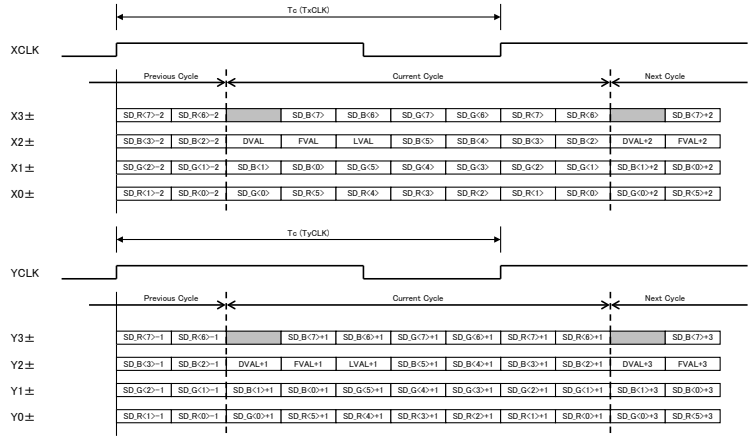
(1) When the internal sync. mode is set, even if an external sync. signal is input, it will not be accepted. This Product operates only with the sync. signal generated internally.

(2) When pixel interpolation is ON, the maximum line speed will be down due to the increase in the number of internal processing pixels. Please refer to the Data Sheet (TM-XK610) for the details of the scanning speed.

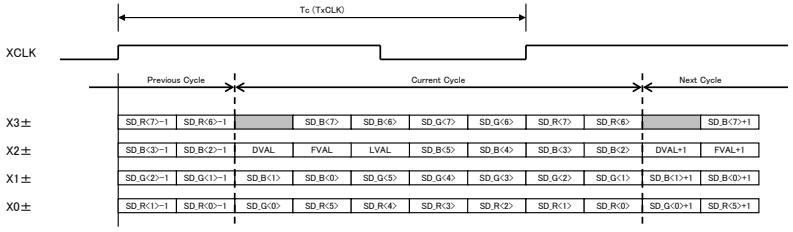
4-7 Data Output

4-7-1 Data Output Format 1

A. 24bit-RGBColor × 2tap（Camera Link™ compliant）
Medium Configuration



B-1. 24bit-RGBColor × 1tap No.1
（Camera Link™ compliant）
Base Configuration



This product can switch between 4 types of Data Output Formats.
（Refer to “5-2 Setting 2 output format setting. “）

A. 24bit-RGBColor × 2tap（Camera Link™ compliant）

(1) This Configuration is an output mode that can output 2 pixels of ODD / EVEN at once with 8 bits for each RGB color.

2）It is a format that outputs 2 pixels from 2 ports based on the Base Configuration output.
(Compliant with Camera Link ™ Specification-v2.1)
Using this format, the fastest line period of 44us / Line (excluding A3+, resolution 600dpi, when pixel interpolation is OFF) can be output.

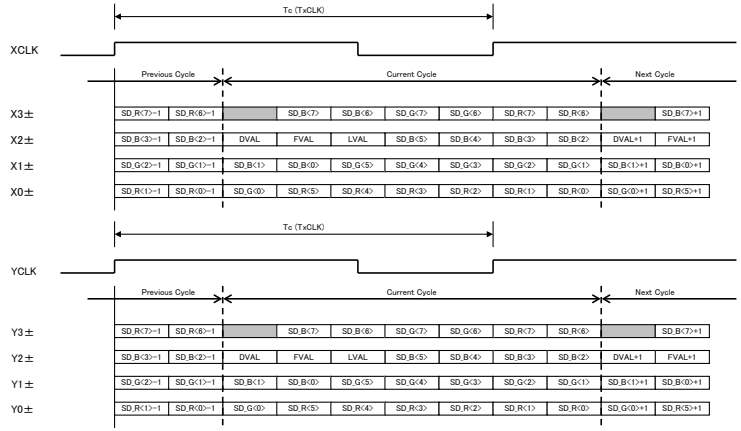
B-1. 24bit-RGBColor × 1tap No.1
（Camera Link™ compliant）

(1) The standard output mode of 24bit-RGBColor .
(8bit for each RGB color.)

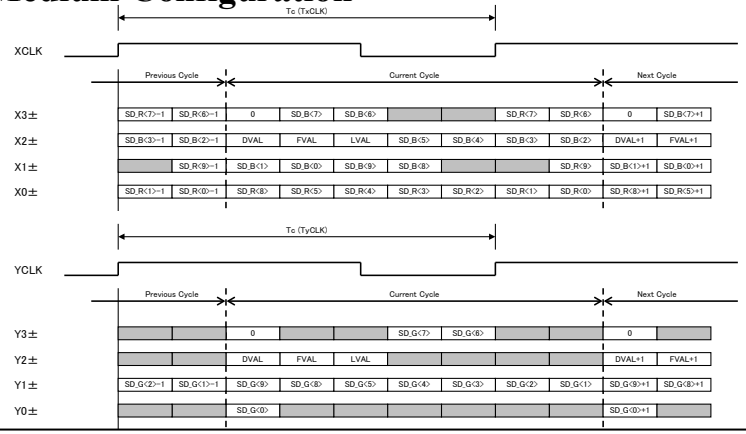
4-7 Data Output

4-7-2 Data Output Format 2

B-2. 24bit-RGBColor × 1tap No.2
（Original Configuration）
Base Configuration × 2



C. 30bit-RGBColor（ Camera Link™ compliant ）
Medium Configuration



B-2. 24bit-RGBColor × 1tap②
（Original Configuration）

(1) The standard output mode of 24-bit-RGB color (8bit for each RGB color).
The difference from No. 1 is that the same image is output from the two connectors in the same format. Please use it when you want to check the image on the user side at the same time as acquiring it with the control device for testing etc.

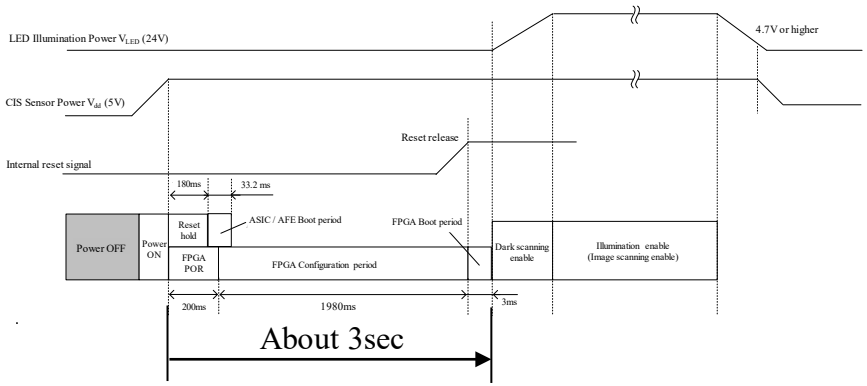
C. 30bit-RGBColor（ Camera Link™ compliant ）

(1) The output mode shown on the left is supported as the 10-bit mode for each RGB color.

(2) This format conforms to the Medium Configuration Camera Link™ specifications with a gradation depth of 10 bits.

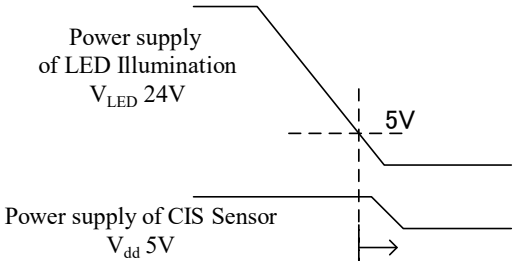
4-8 Recommended sequence for power up / down

4-8-1 Recommended Turn ON sequence



After turning on the 5V power supply,
Dark image output can be captured in about 3 sec.
Ultimately, judge whether the image can be captured by the Status LED blinking green.

4-8-2 Recommended Turn OFF sequence



There is no problem with 5V and 24V turning off at the same time.
If anything, it is recommended to turn off the 5V power supply after turning off the 24V power supply and wait until it becomes 5V or less.

[Recommended Turn ON sequence]

(1) Recommended to turn on the power supply at the timing shown on the left.

(2) If the power supply can be controlled, wait at least 3 sec after V_{dd} 5V rises (5V power supply is 4.75V or more), and then turn on V_{LED} 24V. Initialization is completed about 3 sec after the power is turned on.
Even if V_{dd} 5V and V_{LED} 24V are turned on at the same time, they will not be damaged or malfunction. However, don't apply only V_{LED} 24V power supply for a long time. The illumination and illumination drive may generate heat, resulting in failure.

(3) Whether the initialization is completed or not
User can check by reading XBOOT of Status Register.
For details, refer to "5-2 (Other) Software Boot 1 to 4".

[Recommended Turn OFF sequence]

(1) Turn off the power after ending the communication control.

(2) Recommended to turn off the power supply at the timing shown on the left.
* If control is possible, it is recommended to turn off V_{dd} 5V when the voltage level of the V_{LED} 24V power supply is 5V or less. Even if it is turned off at the same time, it will not be damaged or malfunction.

[Notice]

(1) Each timing depends on the power supply performance user has prepared. Please use after confirming the turn ON / OFF timing at the time of evaluation

(2) If you apply 5V and 24V at the same time, the LED illuminations may shine brightly for a moment, but it will not damage or failure of this product.

(3) If no image data is output after turning on the power, try turning the power off and on again.

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Changes for the Better

Chapter 5 : Getting started

5-1 Initial settings

5-1-1 Initial setting (Factory default)

When the power is turned on or
Settings when both ASIC and FPGA are software boot

Item	Initial setting
1. Output Camera Link™ Clock Freq.	84 MHz
2. Output Camera Link™ Configuration	24bit-RGB Base Configuration
3. Resolution Selecting	600dpi
4. Line Sync Input	Select external sync Signal input
5. Output Width Setting	・Sensor pixel output start position - No offset ・Number of effective output pixels A3/A1/A0 : 7296pixels A3+ : 7904pixels
6. Dark Correction	OFF (Invalid)
7. LED Illumination Control and Setting ※illumination less products (NL series) cannot be used.	Turn on （After inputting Sync signal） Period on illumination : 37.5usec
8. White Correction	OFF (Invalid)
9. PGA	1x
10. Interpolation	OFF (Invalid)
11. Overlap Output	OFF (Invalid)
12. Line Adjustment	ON (Valid), Transport direction in the scanning direction : KDAX4 normal direction （B → G → R : B-line first）
13. γ Correction	OFF (Invalid)

[CIS initial settings]

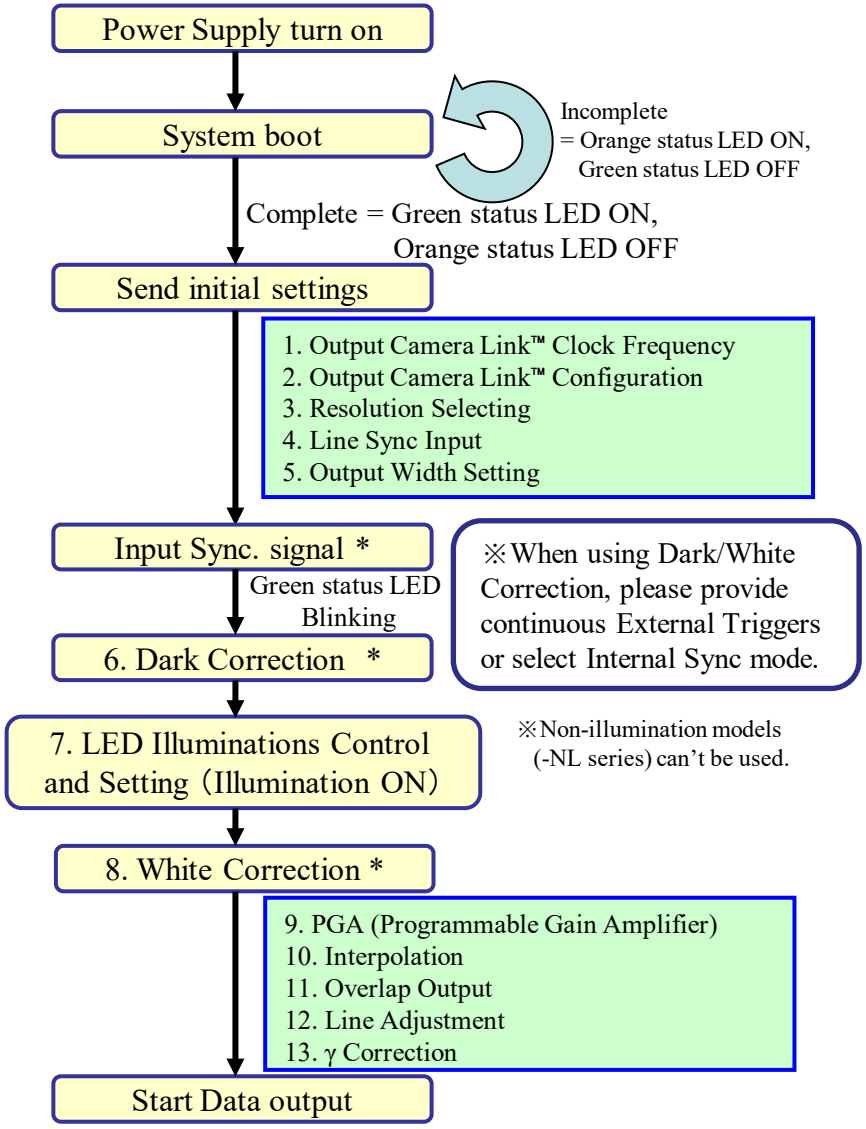
(1) This product operates in the state shown in the table on the left when the power supply is turned on in the factory default state.
(2) Immediately after the power is turned on, this product will be in the following state.
・Scanning image output from CIS :
Output starts after the external sync signal is input.
* However, the image will be valid only after about 10 lines of continuous input of sync signal.
・Illuminations（LED）:
- Immediately after the power is turned on, the illuminations are off.
-After external sync signal input, the illuminations start on.
(3) For individual settings according to the intended use, refer to the explanations on the following pages.

[Notice]
IF the image data is not output from CIS after the power is turned on, please check the following.
(1) Is a synchronization signal input?
(2) Is the voltage range of the power supply voltage justified? (4.75-5.5V on CIS connector)
(3) If there is no problem with the above, try turning the power off and on again.

5-2 Procedure of function settings

※ Refer to "Appendix A-3: Register List" for a register addresses' list.

5-2-1 Procedure of function settings



[Procedure of function settings]

(1) This product contains several image processing function that can be controlled over Serial Communication (UART) via Camera Link™.

(2) Procedure of several function settings is described on the left chart. Change each respective settings for your applications.

1. Output Camera Link™ Clock Frequency
2. Output Camera Link™ Configuration
3. Resolution Selecting
4. Line Sync Input
5. Output Width Setting
6. Dark Correction *
7. LED Illuminations Control and Setting
   ※Non-illumination models (-NL series) can't be used.
8. White Correction *
9. PGA (Programmable Gain Amplifier)
10. Interpolation
11. Overlap Output
12. Line Adjustment
13. γ Correction

Image scanning settings are completed with the above steps 1 to 13.

(3) For adjustments that correspond to changes over time, see the changes in the signal status of this product before setting.

(4) This product is possible to overwrite the value in EEPROM and save the setting for the function (Dark and White correction value) with a large amount of data transfer by setting each time. Please refer to the function specification for the setting method. (However, since our factory settings will be rewritten, please take sufficient precautions such as storing the initial values separately.)

[Notice]

- **For Dark and White correction, input the sync signal continuously from the outside or perform in the internal sync. mode.**
- **For Dark and White correction, it is recommended to generate data for each scan.**

5-2 Setting 1 : Output Camera Link™ Clock Frequency

5-2-2 Output Camera Link™ Clock Frequency

※ As described on page 53, in this document, all numerical values with "h" or "0x" are equally hexadecimal.
"0x" notation for register is the addresses and commands and "h" notation is the register setting values .

[Settings]

Command setting destination : FPGA (Example :0xB2 ALL FPGA)

Address	Register Name	Function
0x0118	OCLK_SEL	Set Camera Link™ Clock Frequency "0"(00h) 48MHz ～"28"(1Ch) 84MHz To select the Camera Link™ output clock frequency, refer to the frequency correspondence table below.

[Register Map]

	b7	b6	b5	b4	b3	b2	b1	b0
0x0118				OCLK_SEL				

[The frequency correspondence table]

Setting Value	Output Frequency (MHz)	Setting Value	Output Frequency (MHz)	Setting Value	Output Frequency(MHz)
0 (00h)	48.0	11 (0Bh)	57.6	22 (16h)	72.0
1 (01h)	50.7	12 (0Ch)	58.3	23 (17h)	76.0
2 (02h)	51.0	13 (0Dh)	60.0	24 (18h)	76.8
3 (03h)	51.4	14 (0Eh)	61.7	25 (19h)	78.0
4 (04h)	52.0	15 (0Fh)	62.4	26 (1Ah)	80.0
5 (05h)	52.8	16 (10h)	64.0	27 (1Bh)	81.6
6 (06h)	53.3	17 (11h)	65.1	28 (1Ch)	84.0
7 (07h)	54.0	18 (12h)	66.0	29 (1Dh)	84.0
8 (08h)	54.9	19 (13h)	67.2	30 (1Eh)	84.0
9 (09h)	56.0	20 (14h)	68.0	31 (1Fh)	84.0
10 (0Ah)	57.0	21 (15h)	68.6		

※ Please note that the output Camera Link™ Clock frequency will be 84.0MHz when the setting value 29 (1Dh) to 31 (1Fh) is input.

[Setting Output Camera Link™ Clock Frequency]

[Function] Sets the frequency of the pixel clock output from the Camera Link™ connector.

[Initial Setting] 84MHz **（0x0118= 1Ch)**

[Adjustable range] 29 types from 48MHz to 84MHz
（See the table on the left for the frequencies that can be set.）

[Example setting]
For 84MHz, write the set value 1Ch to the register address 0x0118 for ALL FPGA (0xB2).

[Notice]

(1) The output Camera Link™ clock frequency and Line scan frequency must satisfy the following relationship.
Where Line scan frequency (kHz) = 1 / Line period (μsec)
1. In case of Base Configuration
Camera Link™ clock frequency(MHz) ＞ 7,400 × Line scan frequency(kHz)
2. In case of Medium Configuration
Camera Link™ clock frequency(MHz) ＞ 7,400 × Line scan frequency(kHz)/2
(Example) Base Configuration : Camera Link™ clock frequency＝70MHz
70MHz / 7400 ＝9.5kHz(≒ 1 / 105μsec/Line)
The above is the fastest Line scan frequency.

(2) For details on control, also check the function specification.

(3) Recommend that you don't write the set values 29 (1Dh) to 31 (1Fh).
（May cause confusion about settings when using）

Example of Communication Command

Setting of 84MHz
0x1B 0xB2 0x00 0x04 0x02 0x01 0x18 0x1C 0xFF

5-2 Setting 2 : Output Camera Link™ Configuration

5-2-3 Output Camera Link™ Configuration

[Settings]
Command setting destination : FPGA (Example :0xB2 ALL FPGA)

Address	Register Name	Function
0x0120	DATA_FORM	Camera Link ™ output format switching “0” (00h) (Type B-1) 24bit-RGB No.1 (Base Configuration) “1” (01h) (Type B-2) 24bit-RGB No.2 (Base Configuration x 2) “2” (02h) (Type A) 24bit-RGB x 2 (Medium Configuration) “3” (03h) (Type C) 30bit-RGB(Medium Configuration)

[Register Map]

	b7	b6	b5	b4	b3	b2	b1	b0
0x0120							DATA_FORM	

- For details on the Camera Link™ output format, refer to the next page and the Data Sheet.

[Select the Camera Link™ Configuration]

[Function] Selects the format of the image output configuration the Camera Link™ connector.
[Initial Setting] **0x0120= 00h**
Type B-1 : 24bit-RGB(Base Configuration)
[Setting mode]
Type A : 24bit-RGB x 2(Medium Configuration)
Type B-1 : 24bit-RGB No.1(Base Configuration)
Type B-2 : 24bit-RGB No.2(Base Configuration x 2)
Type C : 30bit-RGB(Medium Configuration)

[Notice]
(1) The output configurations, Line period, and Camera Link clock frequency are related to each other, so please calculate each setting before using.

(2) When changing this setting, also change the setting on the Frame Grabber.

Example of Communication Command

(Type A) 24bit-RGB x 2 (Medium Configuration)
0x1B 0xB2 0x00 0x04 0x02 0x01 0x20 0x02 0xFF
(Type B No.1) 24bit-RGB No.1 (Base Configuration)
0x1B 0xB2 0x00 0x04 0x02 0x01 0x20 0x00 0xFF
(Type C) 30bit-RGB (Medium Configuration)
0x1B 0xB2 0x00 0x04 0x02 0x01 0x20 0x03 0xFF

5-2 Setting 2 : Output Camera Link™ Configuration

5-2-4 Details of Output configuration

(Type A)24bit-RGB x 2 (Medium Configuration)

Port/bit	24-bit RGB*2tap	
Port A0	R0	ODD
Port A1	R1	ODD
Port A2	R2	ODD
Port A3	R3	ODD
Port A4	R4	ODD
Port A5	R5	ODD
Port A6	R6	ODD
Port A7	R7	ODD
Port B0	G0	ODD
Port B1	G1	ODD
Port B2	G2	ODD
Port B3	G3	ODD
Port B4	G4	ODD
Port B5	G5	ODD
Port B6	G6	ODD
Port B7	G7	ODD
Port C0	B0	ODD
Port C1	B1	ODD
Port C2	B2	ODD
Port C3	B3	ODD
Port C4	B4	ODD
Port C5	B5	ODD
Port C6	B6	ODD
Port C7	B7	ODD

Port/bit	24-bit RGB*2tap	
Port D0	R0	EVEN
Port D1	R1	EVEN
Port D2	R2	EVEN
Port D3	R3	EVEN
Port D4	R4	EVEN
Port D5	R5	EVEN
Port D6	R6	EVEN
Port D7	R7	EVEN
Port E0	G0	EVEN
Port E1	G1	EVEN
Port E2	G2	EVEN
Port E3	G3	EVEN
Port E4	G4	EVEN
Port E5	G5	EVEN
Port E6	G6	EVEN
Port E7	G7	EVEN
Port F0	B0	EVEN
Port F1	B1	EVEN
Port F2	B2	EVEN
Port F3	B3	EVEN
Port F4	B4	EVEN
Port F5	B5	EVEN
Port F6	B6	EVEN
Port F7	B7	EVEN

(Type B-1)24bit-RGB No.1 (Base Configuration)

Port/bit	24-bit RGB
Port A0	R0
Port A1	R1
Port A2	R2
Port A3	R3
Port A4	R4
Port A5	R5
Port A6	R6
Port A7	R7
Port B0	G0
Port B1	G1
Port B2	G2
Port B3	G3
Port B4	G4
Port B5	G5
Port B6	G6
Port B7	G7
Port C0	B0
Port C1	B1
Port C2	B2
Port C3	B3
Port C4	B4
Port C5	B5
Port C6	B6
Port C7	B7

(Type B-2)24bit-RGB No.2 (Base Configuration x 2)

Port/bit	24-bit RGB
Port A0	R0
Port A1	R1
Port A2	R2
Port A3	R3
Port A4	R4
Port A5	R5
Port A6	R6
Port A7	R7
Port B0	G0
Port B1	G1
Port B2	G2
Port B3	G3
Port B4	G4
Port B5	G5
Port B6	G6
Port B7	G7
Port C0	B0
Port C1	B1
Port C2	B2
Port C3	B3
Port C4	B4
Port C5	B5
Port C6	B6
Port C7	B7

Port/bit	24-bit RGB
Port D0	R0
Port D1	R1
Port D2	R2
Port D3	R3
Port D4	R4
Port D5	R5
Port D6	R6
Port D7	R7
Port E0	G0
Port E1	G1
Port E2	G2
Port E3	G3
Port E4	G4
Port E5	G5
Port E6	G6
Port E7	G7
Port F0	B0
Port F1	B1
Port F2	B2
Port F3	B3
Port F4	B4
Port F5	B5
Port F6	B6
Port F7	B7

(Type C) 30bit-RGB(Medium Configuration)

Port/bit	30-bit RGB
Port A0	R0
Port A1	R1
Port A2	R2
Port A3	R3
Port A4	R4
Port A5	R5
Port A6	R6
Port A7	R7
Port B0	R8
Port B1	R9
Port B2	nc
Port B3	nc
Port B4	B8
Port B5	B9
Port B6	nc
Port B7	nc
Port C0	B0
Port C1	B1
Port C2	B2
Port C3	B3
Port C4	B4
Port C5	B5
Port C6	B6
Port C7	B7

Port/bit	30-bit RGB
Port D0	nc
Port D1	nc
Port D2	nc
Port D3	nc
Port D4	nc
Port D5	nc
Port D6	nc
Port D7	nc
Port E0	G0
Port E1	G1
Port E2	G2
Port E3	G3
Port E4	G4
Port E5	G5
Port E6	G6
Port E7	G7
Port F0	G8
Port F1	G9
Port F2	nc
Port F3	nc
Port F4	nc
Port F5	nc
Port F6	nc
Port F7	nc

5-2 Setting 3 : Resolution Selecting

5-2-5 Resolution Selecting

[Settings]

Command setting destination : FPGA (Example :0xB2 ALL FPGA)

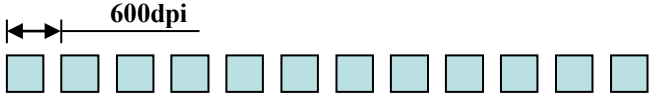
(Command setting details: P60 4-4-3 Refer to the command list.)

Address	Register Name	Function
0x0124	RESOLUTION	Select the resolution of the output images. "0"(00h) 600dpi , "1"(01h) 300dpi "2"(02h) 200dpi , "3"(03h) 150dpi

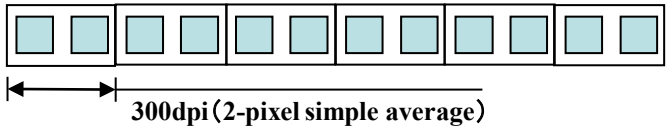
[Register Map]

	b7	b6	b5	b4	b3	b2	b1	b0
0x0124							RESOLUTION	

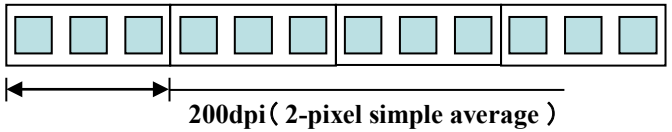
(1) Pixel combination at 600dpi



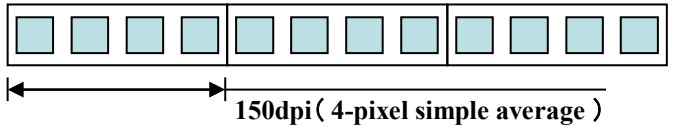
(2) Pixel combination at 300dpi



(3) Pixel combination at 200dpi



(4) Pixel combination at 150dpi



[Resolution Selecting]

[Function] Select the resolution of the image.

[Initial Setting] 600dpi **(0x0124 = 00h)**

[Setting mode]

4 types of Resolution : 150dpi、200dpi、300dpi、600dpi

[Notice]

(1) The Sensor (photodiode) IC resolution of the reader is 600dpi. Resolution conversion is performed in the data output section after all signal processing is completed.

(2) The resolution conversion performs the following.
- 300dpi mode Average the data of 2 adjacent pixels.
- 200dpi mode Average the data of 3 adjacent pixels.
- 150dpi mode Average the data of 4 adjacent pixels.

(3) The resolution of the Sensor IC is 600dpi, but it has a function that can speed up the maximum Line cycle when the resolution is small.
In addition, the read clock frequency can be reduced according to the resolution.

(4) If user lower the resolution, change the relative scan speed of the scanning medium according to the resolution.
- At 150dpi, 4 times as much as 600dpi,
- At 200dpi, 3 times as much as 600dpi,
- At 300dpi, 2 times as much as 600dpi

Example of Communication Command

Resolution 600dpi mode

0x1B 0xB2 0x00 0x04 0x02 0x01 0x24 0x00 0xFF

Resolution 300dpi mode

0x1B 0xB2 0x00 0x04 0x02 0x01 0x24 0x01 0xFF

Resolution 200dpi mode

0x1B 0xB2 0x00 0x04 0x02 0x01 0x24 0x02 0xFF

5-2 Setting 4 : Line Sync Input

5-2-6 Line Sync Input

[Settings]

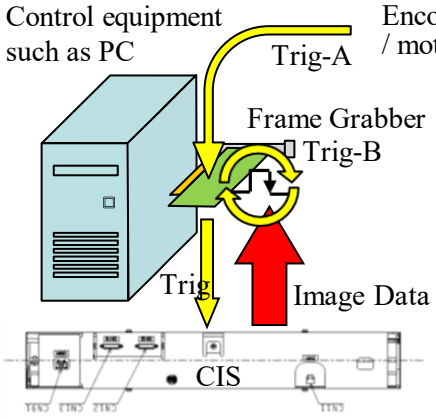
Command setting destination : FPGA (Example :0xB2 ALL FPGA)

Address	Register Name	Function
0x01A0	EXTSYNC	Select sync. mode "0"(00h) Internal Sync. mode "1"(01h) External Sync. mode
0x01A1 0x01A2	H_CYCLE	Line cycle setting in internal sync. Mode. (Example) At 44µse/line, set **0E6Fh(3,695).** → 0x01A1 6Fh, 0x01A2 0Eh Camera Link™ clock freq. 84MHz 3,696÷84=44

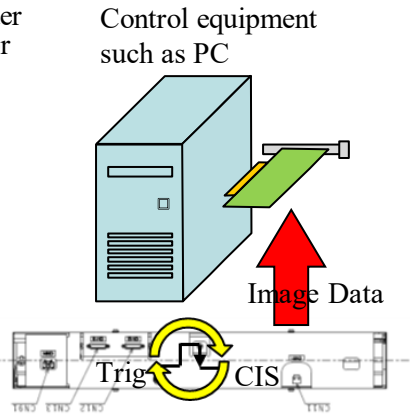
[Register Map]

	b7	b6	b5	b4	b3	b2	b1	b0
0x01A0								EXT SYNC
0x01A1	H_CYCLE(7:0)							
0x01A2	H_CYCLE(15:8)							

[External sync. (Trig) mode]



[Internal sync. mode]



[Setting Line Sync.]

[Function] Sets the sync signal input source and internal sync. signal Line period.

[Initial Setting] External Sync. mode **(0x01A0 = 01h)**

This mode allows user to input a Line sync. signal from the outside through the Camera Link™ I / F (CC1).

[Setting mode]

External sync. (Trig) mode ／Internal sync.（Free run）mode

[Notice]

(1) Due to the internal delay after the start of scanning, the 10 lines immediately after the sync. signal input will not be output as correct scanning image data.
（Especially, be careful when scanning intermittently to stop the sync. signal.）

(2) In the external sync. mode, this product is necessary to input the Line sync. signal according to the scanning frequency. Enter the sync. signal that matches the transport speed of the medium to be scan or the CIS.

(3) In the internal synchronization mode, a sync. signal with a fixed cycle is generated inside the CIS. The following formula is based on the Camera Link ™ frequency.

$$\text{Setting Line cycle (µsec)} = \frac{\text{(Register setting value + 1)}}{\text{Camera Link™ Frequency(MHz)}}$$

Example of Communication Command

External Sync. mode

0x1B 0xB2 0x00 0x04 0x02 0x01 0xA0 0x01 0xFF

Internal Sync. mode : Example 1 44µsec/line(22.7kHz)

0x1B 0xB2 0x00 0x05 0x02 0x01 0xA1 0x6F 0x0E 0xFF

0x1B 0xB2 0x00 0x04 0x02 0x01 0xA0 0x00 0xFF

Internal Sync. mode : Example 2 88µsec/line(11.3kHz)

0x1B 0xB2 0x00 0x05 0x02 0x01 0xA1 0xDF 0x1C 0xFF

0x1B 0xB2 0x00 0x04 0x02 0x01 0xA0 0x00 0xFF

5-2 Setting 5 : Output Width Setting

5-2-7 Sensor pixel output start position offset and number of effective output pixels setting

[Settings]

Command setting destination : FPGA (Example :0xB2 ALL FPGA)

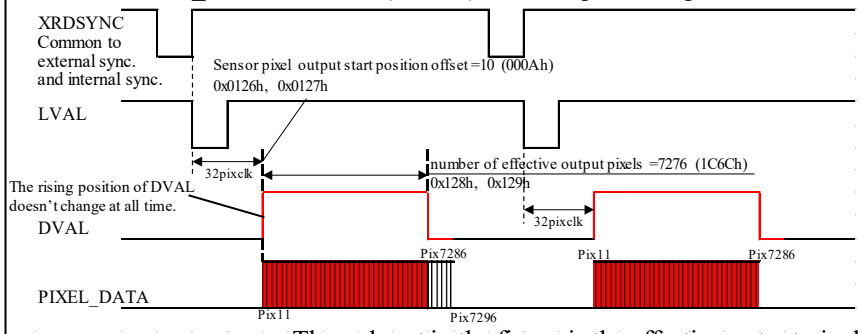
Address	Register Name	Function
0x0126 0x0127	OUT_ XOFFSET	Offsets the output start position of the sensor pixels. The output start position is offset by the set value.
0x0128 0x0129	OUT_ WIDTH	Set the number of valid output pixels from the pixels set by OUT_XOFFSET.

[Register Map]

	b7	b6	b5	b4	b3	b2	b1	b0
0x0126	OUT_XOFFSET(7:0)							
0x0127				OUT_XOFFSET(12:8)				
0x0128	OUT_WIDTH (7:0)							
0x0129				OUT_WIDTH (12:8)				

[Output pixel timing chart example (for A3 size)]

Example: When OUT_XOFFSET = 10 (000Ah)
and OUT_WIDTH = 7276 (1C6Ch) for 7296 pixels output



The red part in the figure is the effective output pixels.

[Output Width Setting]

[Function] For changing the settings, the output start position of the output pixel and the number of effective output pixels can be set.

[Initial Setting] Sensor pixel output start position offset.
OUT_XOFFSET = 0000h
Number of effective output pixels.
A3/A1/A0 7296 (OUT_WIDTH = 1C80h)
A3+ 7904 (OUT_WIDTH = 1EE0h)

[Setting mode]
Sensor pixel output start position offset.
(Set value range: 0000h～1FFFh)
Number of effective output pixels.
(Set value range: 0000h～1FFFh)

[Notice]

(1) When you change the pixel interpolation, overlap, or resolution settings, change the number of effective output pixels with WIDTH according to the required number of pixels.

(2) The OUT_XOFFSET value should be shorter than the maximum number of pixels determined by the external sync. or internal sync. signal. If it is long, the image may not be output.

(3) The sum of the OUT_XOFFSET value and the OUT_WIDTH value should be shorter than the maximum number of pixels determined by the external sync. or internal sync. signal. If it is long, the image may not be output.

Example of Communication Command

Sensor pixel output start position offset. 10pix (000Ah)
0x1B 0xB2 0x00 0x05 0x02 0x01 0x26 0x0A 0x00 0xFF

By setting Parameter Size to 0x05
Writing to two consecutive addresses is possible.

Number of effective output pixels. 7276pix (1C6Ch)
0x1B 0xB2 0x00 0x05 0x02 0x01 0x28 0x6C 0x1C 0xFF

5-2 Setting 6 : Dark Correction

※ At the time of Dark correction, turn off the illuminations and input the sync. signal continuously from the External or Internal sync. mode.
Dark Correction is based on the calculated value from the continuously acquired multiple line images,
so if continuous multiple line images can't be acquired, can't get the correct Dark Correction.

5-2-8 Dark Correction

[Settings]

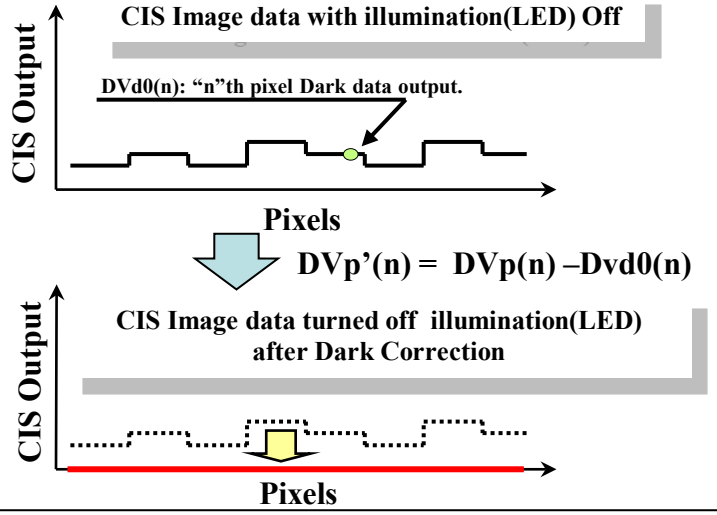
Command setting destination : ASIC (Example :0xA2 ALL ASIC)

Address	Register Name	Function
0x0342	D_SHADING_SET	Automatic generate Dark Correction Data. Generated trigger ON by "0" → "1".
0x0375	R/G/B_DARK_ ENB	Dark Correction ON / OFF control for each color of R / G / B "0" OFF, "1" ON

[Register Map]

	b7	b6	b5	b4	b3	b2	b1	b0
0x0342								D_SHADING_SET
0x0375						R_DARK_ENB	G_DARK_ENB	B_DARK_ENB

[Conceptual diagram of Dark Correction function]



[Dark Correction]

[Function] Corrects the offset variation of each pixel of Dark output.
[Initial Setting] Dark Correction OFF **(0x0375= 00h)**
[Setting mode] 1. Generating of Dark correction data
2. Dark Correction ON/OFF

* After the status of address changes "0x0342-b0" → "0" , it will start to generate Dark Correction. Don't change the value of other bits of 0x0342.
* Each bit of address 0x0375 specifies whether Dark Correction is applied to each signal of b2-R, b1-G, and b0-B.

[Notice]

(1) Initial Dark Correction data is stored in the CIS at the time of shipment from the factory, and the data is automatically loaded when CIS's power is turned on.
(2) The Dark output of the sensor fluctuates depending on the temperature, scan rate, etc. According to the application, recreate the Dark Correction data at appropriate intervals according to the application.
(3) If Dark Correction isn't performed correctly, streaky fluctuations may appear in the scanning images.
(4) Use the White Correction after enabling the Dark Correction.
(5) Refer to "Appendix A-3" in this document for a list of addresses.

Example of Communication Command

Automatic generating Dark Correction Data start.
0x1B 0xA2 0x00 0x04 0x02 0x03 0x42 0x00 0xFF
0x1B 0xA2 0x00 0x04 0x02 0x03 0x42 0x01 0xFF
Dark Correction ON
0x1B 0xA2 0x00 0x04 0x02 0x03 0x75 0x07 0xFF
Dark Correction OFF
0x1B 0xA2 0x00 0x04 0x02 0x03 0x75 0x00 0xFF

5-2 Setting 7-1 :
LED Illuminations Control and Setting

※ -NL series is not available. Refer to the Data Sheet for the usage conditions of the external illuminations for –NL series.

5-2-9 LED illuminations setting procedure

[Settings]

Command setting destination : ASIC (Example :0xA2 ALL ASIC)

Address	Register Name	Function
0x030C	LED_CONT _ENB	Select illumination mode “0” (00h) Illumination OFF. “4” (04h) One side illumination(B) ON. Lower-stream side illumination(B) ON. “8” (08h) One side illumination(A) ON. Upper-stream side illumination(A) ON. “12” (0Ch) Both side illuminations ON. Upper-stream side illumination(A) and Lower-stream side illumination(B) ON.

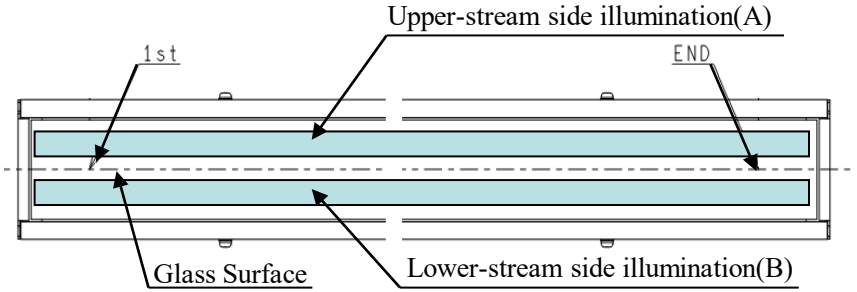
[Register Map]

Fixed to “0”

	b7	b6	b5	b4	b3	b2	b1	b0
0x030C					LED_CONT _ENB		0	0

* “1” is the illumination On.
* b3 is Upper-stream side illumination(A) and b2 is Lower-stream side illumination(B).
* Always fix b0 and b1 to "0".

[Conceptual diagram of illuminations arrangement]



[LED illumination Control]

[Function] * Only can use the product with the built-in illuminations.
Control the LED illuminations Settings.

[Initial Setting] Both side illuminations On. **(0x030C= 0Ch)**

[Setting mode]

1. Both side illuminations On mode.
2. Lower-stream side illumination(B) ON.
3. Lower-stream side illumination(B) ON.
4. Illumination OFF.

[Notice]

(1) LED illuminations are controlled by Camera Link™ communication. Therefore, the control is asynchronous with the Line sync. signal.

(2) White Correction data can be saved only in one of the illumination modes. When scanning images by switching between multiple modes and illuminations, internal White Correction is not possible.

Example of Communication Command

Both side illuminations On.
0x1B 0xA2 0x00 0x04 0x02 0x03 0x0C 0x0C 0xFF

One side illumination(A) ON.
0x1B 0xA2 0x00 0x04 0x02 0x03 0x0C 0x08 0xFF

One side illumination(B) ON.
0x1B 0xA2 0x00 0x04 0x02 0x03 0x0C 0x04 0xFF

Illumination OFF.
0x1B 0xA2 0x00 0x04 0x02 0x03 0x0C 0x00 0xFF

5-2 Setting 7-2 : LED illumination Control（Duty setting）

※ -NL series is not available. Refer to the Data Sheet for the usage conditions of the external illuminations for –NL series.

5-2-10 LED illumination lighting period setting

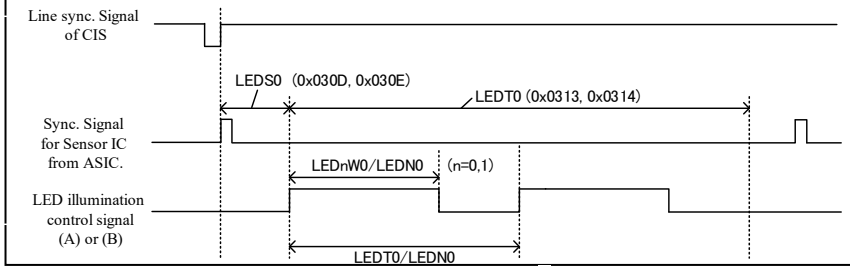
[Settings]

Command setting destination : ASIC (Example :0xA2 ALL ASIC)

Address	Register Name	Function
0x030F 0x0310	LED0W0	Lower-stream side illumination(B) period setting. Example） In the case of 37.5 µs, common to illumination (A) and (B) 37.5 µs / 29.15 ns ≒ 1287 (Decimal number, rounded up) Hexadecimal conversion 0x030F 07h, 0x0310 05h
0x0311 0x0312	LED1W0	Upper-stream side illumination(A) period setting.
0x0313 0x0314	LEDT0	Set illuminations effective period. Initial value 63353(FFFFh)
0x030D 0x030E	LEDS0	Set illumination lighting start position. **（Do not change this register from the initial value because it matches the image scanning timing of the sensor IC.）** Initial value 34 (0022h)
0x032D	LEDN0	Set illumination Pulse division. “0”(00h) OFF “1”(01h) 2pulse “2”(02h) 4pulse “3”(03h) 8pulse ”4”(04h) 16pulse

*Illumination lighting period ≒ Register set value (decimal number) x 29.15 nsec

[LED control signal output timing chart]



[LED illumination lighting period control]

* Only can use the product with the built-in illuminations.

[Function] Adjust the illumination lighting period.

[Initial Setting] Pulse division OFF **(0x032D = 00h)**

***The lighting pulse period is the factory adjustment setting value.**

[Setting mode] The following settings are available.

1. Illumination lighting pulse period setting.
2. Illumination pulse division. 1 / 2 / 4 / 8 pulse.

[Notice]

(1) Set the same values for LED0W0 (0x030F, 0x3010) and LED1W0 (0x0311, 0x0312) as much as possible.
If different values are entered, the lighting balance of the two illuminations will be lost.

(2) For multi-pulse illumination, scan the LEDT0 (0x0313, 0x0314) value and set a period with a margin for fluctuations in the Line cycle.

(3) Refer to the Function Specifications for the details of the multi-pulse illumination.

(4) If the illuminations effective period (LEDT) setting is longer than the CIS line cycle, it will be reset at the start of the next line.

Example of Communication Command

Pulse lighting period when 37.5 µsec is set.
From 37.5 µsec / 29.15nsec ≒ 1287 (0507h), write 07h to register addresses 0x030F and 0x0311, and write 05h to 0x0310 and 0x0312.

0x1B 0xA2 0x00 0x05 0x02 0x03 0x0F 0x07 0x05 0xFF
0x1B 0xA2 0x00 0x05 0x02 0x03 0x11 0x07 0x05 0xFF

5-2 Setting 8-1 : White Correction

※ When White Correction, turn on the Dark Correction and input the sync. signal continuously from the External or Internal sync. mode.
White Correction is based on the calculated value from the continuously acquired multiple line images,
if continuous multiple line images can't be acquired, can't get the correct White Correction.

5-2-11 White Correction 1

[Settings]

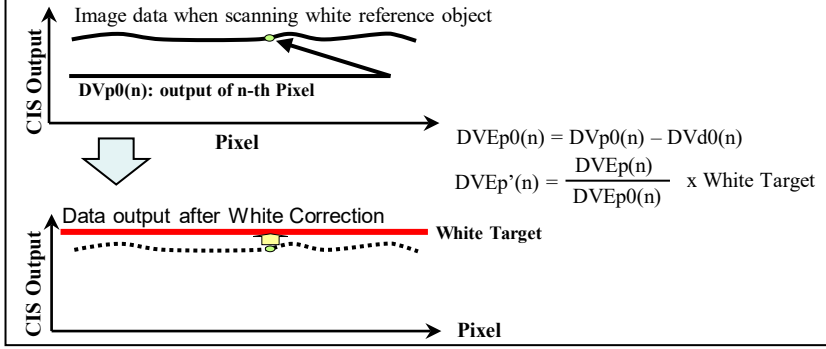
Command setting destination : ASIC (Example :0xA2 ALL ASIC)

Address	Register Name	Function
0x0342	W_SHADING_SET	Normal mode White correction data generation trigger (bit b1). Trigger ON by transition "0" → "1".
0x0396	R/G/B_WHITE_ENB	When W_COL_MODE = "0" (see next page). White Correction ON / OFF control for each color of R / G / B. b2-R, b1-G, b0-B each signal "0" OFF, "1" ON
0x03B2	R/G/B_SBSHFF	When W_COL_MODE = "1" (see next page). White Correction ON / OFF control for each color of R / G / B. b2-R, b1-G, b0-B each signal "0" OFF, "1" ON

[Register Map] **Must not change the "0" fixed bit.**

	b7	b6	b5	b4	b3	b2	b1	b0
0x0342					0	0	W_SHADING_SET	0
0x0396		0	0	0		R_WHITE_ENB	G_WHITE_ENB	B_WHITE_ENB
0x03B2		0	0	0		R_SBSHFF	G_SBSHFF	B_SBSHFF

[Conceptual diagram of White Correction function]



[White Correction 1]

[Function] Corrects in illumination intensity and sensitivity variation for each pixel to make the output of all pixels uniform.

Refer to the next page for setting the White Target value for white correction.

[Initial Setting]

- Normal mode White correction data generation trigger **(0x0342= 00h)**
- Normal mode White correction OFF **(0x0396= 00h)**
- Max.Hold mode White correction OFF **(0x03B2= 00h)**

[Setting mode]

1. Normal mode white correction data generation
   *Normal mode White Correction generation automatically outputs a trigger from the ASIC and generates white correction from 32 lines (initial value).
2. Normal mode White Correction ON / OFF
3. Max.Hold mode White Correction ON / OFF

[Notice]

(1) When generating White Correction data, turn on Dark Correction and generate correction data with a uniform reflectance chart.

(2) When generating White Correction, the output image may have vertical streaks due to scratches, stains, dust, etc. on the White Correction reference chart.

Example of Communication Command

Normal mode White Correction data generation start.

0x1B 0xA2 0x00 0x04 0x02 0x03 0x42 0x00 0xFF

0x1B 0xA2 0x00 0x04 0x02 0x03 0x42 0x02 0xFF

Normal mode White Correction ON with RGB

0x1B 0xA2 0x00 0x04 0x02 0x03 0x96 0x07 0xFF

Normal mode White Correction OFF with RGB

0x1B 0xA2 0x00 0x04 0x02 0x03 0x96 0x00 0xFF

5-2 Setting 8-2 : White Correction

※ When White Correction, turn on the Dark Correction and input the sync. signal continuously from the External or Internal sync. mode.
White Correction is based on the calculated value from the continuously acquired multiple line images,
if continuous multiple line images can't be acquired, can't get the correct White Correction.

5-2-12 White Correction 2

[Settings]

Command setting destination : ASIC (Example :0xA2 ALL ASIC)

Address	Register Name	Function
0x0398 0x0399	R_WHITE _TARGET	Set the R White Correction Target value. Setting range: 0-4095, **Initial value: 4000.**
0x039A 0x039B	G_WHITE _TARGET	Set the G White Correction Target value. Setting range: 0-4095, **Initial value: 4000.**
0x039C 0x039D	B_WHITE _TARGET	Set the B White Correction Target value. Setting range: 0-4095, **Initial value: 4000.**
0x030A (b3～b0)	MAX-HOLD	Max.Hold mode White Correction data generation trigger (corresponding to bit b3 to b0). Trigger on at the transition from "2" (0010b) to "0" (0000b) (when bit b4 = 1) (Initial value:15) **(notice) In advance "15"(1111b)→"2"(0010b).**
0x0342 (b3)	W_COL_MODE	Select the White Correction mode. (corresponding to bit b3)

[Register Map]

	b7	b6	b5	b4	b3	b2	b1	b0
0x0398	R_WHITE_TARGET (7:0)							
0x0399					R_WHITE_TARGET (11:8)			
0x039A	G_WHITE_TARGET (7:0)							
0x039B					G_WHOTE_TARGET (11:8)			
0x039C	B_WHITE_TARGET (7:0)							
0x039D					B_WHITE_TARGET (11:8)			
0x030A				1	MAX-HOLD (3: 0)			
0x0342					W_COL_MODE	0	0	0

※Must not change the "0" or "1" fixed bit.

[White Correction 2]

[Function] ・Set the White Target value to Correct in illumination intensity and sensitivity variation for each pixel to make the output of all pixels uniform.

・Generates White Correction in Max.Hold mode.

[Initial Setting] (Refer to the previous page)

White Correction OFF: normal mode white correction trigger.

[Setting mode]

1. Setting R, G, B White Correction Target value.
2. Max.Hold mode white correction generation trigger.

*** How to generate White Correction data in Max.Hold mode**

Generation starts when the status of address 0x030A-b1 changes from "1" to "0" with the address 0x0342-b3 set to "1". When using Max.Hold mode, always set 0x030A-b3, b2, b0 to "0". In order to finish, it is necessary to change the state of address 0x030A-b1 from "0" to "1". **To return to normal mode white correction, be sure to set the setting value of address 0x0342-b3 (W_COL_MODE) to "0". Also, set all 0x030A-b3 to b0 (MAX-HOLD) to "1" (15).**

[Notice]

(1) When generating White Correction data, turn on Dark Correction and generate correction data with a uniform reflectance chart.

(2) When generating White Correction, the output image may have vertical streaks due to scratches, stains, dust, etc. on the White Correction reference chart.

Example of Communication Command

Transition to Max.Hold mode.

0x1B 0xA2 0x00 0x04 0x02 0x03 0x42 0x08 0xFF

0x1B 0xA2 0x00 0x04 0x02 0x03 0x0A 0x12 0xFF

Max.Hold mode White Correction data generation start.

0x1B 0xA2 0x00 0x04 0x02 0x03 0x0A 0x10 0xFF

Max.Hold mode White Correction data generation end.

0x1B 0xA2 0x00 0x04 0x02 0x03 0x0A 0x12 0xFF

5-2 Setting 9 : PGA

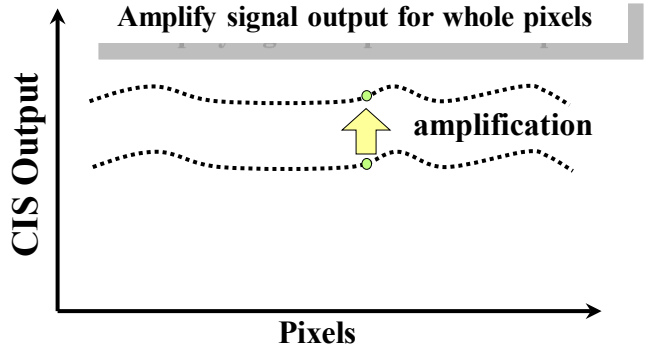
5-2-13 PGA設定

[Settings]

Command setting destination : ASIC (Example :0xA2 ALL ASIC)

Address	Register Name	Function
0x037C	PGA_SW	Set PGA gain ON/OFF. “0”(00h) PGA(gain)OFF “1”(01h) PGA(gain)ON
0x037D 0x037E	REG_R	Set the value of Red PGA. The calculation is based on the right formula. Set the sign with b4 of 0x037E. “0”:+, “1”: - Settable range From -1024 (1400h) to 3071 (0BFFh).
0x037F 0x0380	REG_G	Set the value of Green PGA. The calculation is based on the right formula. Set the sign with b4 of 0x037E. “0”:+, “1”: - Settable range From -1024 (1400h) to 3071 (0BFFh).
0x0381 0x0382	REG_B	Set the value of Blue PGA. The calculation is based on the right formula. Set the sign with b4 of 0x037E. “0”:+, “1”: - Settable range From -1024 (1400h) to 3071 (0BFFh).

[Conceptual diagram of PGA settings]



[PGA（Programmable Gain Amp.）]

[Function] Gains the image signal in scanning line units.

[Initial Setting]

- PGA(gain) OFF **(0x037C = 00h)**
- Set PGA(gain) 1x **(REG_R/G/B= 0000h)**

[Setting mode] 1. Select PGA(gain) ON / OFF
2. 0 - 4.0x magnification adjustment.

The amplification degree for each signal is calculated by the following formula.

$$\text{PGA Output Data} = \frac{1024 + \text{Register value (Decimal Number)}}{1024} \times \text{Input data}$$

[Notice]

(1) When changing the amplification degree of each color, pay attention to the white balance when scanning the color.

Example of Communication Command

PGA ON

0x1B 0xA2 0x00 0x04 0x02 0x03 0x7C 0x01 0xFF

PGA OFF : Image data output without PGA.

0x1B 0xA2 0x00 0x04 0x02 0x03 0x7C 0x00 0xFF

Set the red PGA to the setting value 1024(400h). PGA 2x.

0x1B 0xA2 0x00 0x05 0x02 0x03 0x7D 0x00 0x04 0xFF

By setting Parameter Size to 0x05
Writing to two consecutive addresses is possible.

Address 0x37D

Address 0x37E

5-2 Setting 10 : Interpolation

5-2-14 Interpolation Setting

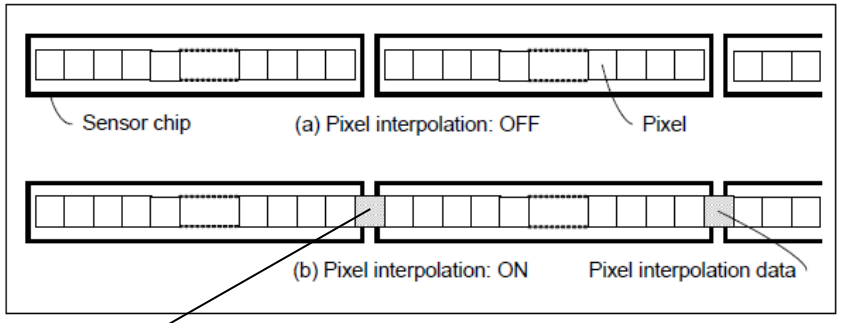
[Settings]
Command setting destination : FPGA (Example :0xB2 ALL FPGA)

Address	Register Name	Function
0x0132	PIX_INTERP_ENB	Set the interpolation ON / OFF. “0”(00h) Interpolation OFF “1”(01h) Interpolation ON

[Register Map]

	b7	b6	b5	b4	b3	b2	b1	b0
0x0132								PIX_INTERP_ENB

[Conceptual diagram of pixel interpolation function]



Possible to fill in the missing pixels between the sensor IC chips by performing interpolation (adding estimated pixels from around the missing pixels). (The interpolated pixel is not the actual read pixel.)

[Pixel interpolation]

[Function] The interpolation is a function to perform pixel interpolation for pixel loss between sensor ICs and A3 modules.
(Refer to the description on page 2-5, page 28.)
[Initial Setting] Interpolation OFF **(0x0132 = 00h)**
[Setting mode] Interpolation ON/OFF

[Notice]

(1) The pixel interpolation is a function that determines the image information around the missing pixel, estimates the pixel information and adds it.
It is not the actual scanning data.
(2) When using this function, please evaluate CIS with the scanned object and judge whether can be adopted or not.
(3) In the case of A0 and A1 size CIS, interpolation between A3 size modules is also performed. In this case, the interpolated pixels between A3 are added at the following positions.
1. In the case of A1, the A3 module output section on the 1st pixel side
2. In the case of A0, the A3 module output section on the 1st pixel side and the center

(4) When interpolation is ON, the fastest scanning speed will be slower due to the increase in the number of internal processing pixels. Refer to the Data Sheet (TM-XL499) for the details of the scanning speed.

Example of Communication Command

Interpolation ON

0x1B 0xB2 0x00 0x04 0x02 0x01 0x32 0x01 0xFF

Interpolation OFF

0x1B 0xB2 0x00 0x04 0x02 0x01 0x32 0x00 0xFF

5-2 Setting 11 : Overlap Output

5-2-15 Overlap Output

[Settings]

Command setting destination : FPGA (Example :0xB2 ALL FPGA)

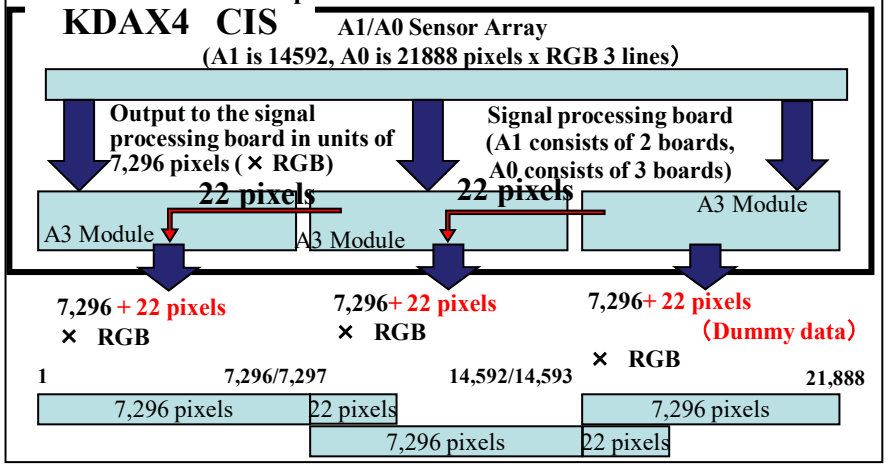
Address	Register Name	Function
0x0123	EXTRA _PIXEL	Set pixel overlap ON / OFF. “0” (00h) Overlap OFF. “1” (01h) Overlap ON.
0x0125	EX_PIXNUM	Select the number of overlap pixels. “0”(00h) : Overlap pixels 22pixels. “1”(01h) : Overlap pixels 84pixels.

[Register Map]

	b7	b6	b5	b4	b3	b2	b1	b0
0x0123								EXTRA _PIXEL
0x0125								EX_ PIXNUM

[Conceptual diagram of overlap output (For 22 pixels)]

By enabling the overlap function,
the data of the first 22 pixels of the next module will be added.



[Overlap Output setting]

[Function]

A1 and A0 size products output image data in parallel in A3 size units, but they can be output in overlaps between A3 units.

Even when importing from multiple PCs, the image near the joint of the A3 unit can be acquired and confirmed correctly.

[Initial Setting]

1. Pixel Overlap OFF **(0x0123 = 00h)**
2. The number of overlap pixels 22pixels **(0x0125 = 00h)**

[Setting mode]

1. Pixel Overlap output ON (valid) / OFF (invalid)
2. The number of overlap pixels. Select 22pixels / 84pixels.

[Notice]

(1) In the case of A1 size, the output of 22 pixels is added to the end of the 1st Module (the leftmost module in the left figure). (In A3 size, 22 pixels are added after 7296 pixels without interpolation, and as a result, 7318 pixels are output.)

The above 22 pixels output is equivalent to the output of the 22 pixels of the 2nd Module. This function is the same for 84 pixels output.

(2) In the case of A0 size, in addition to (1), the data of the first 22 pixels of the 3rd Module is added to the end of the 2nd Module.

The same applies to 84 pixels output.

Example of Communication Command

Overlap output ON.

0x1B 0xB2 0x00 0x04 0x02 0x01 0x23 0x01 0xFF

Number of overlapping pixels 84 pixels selected.

0x1B 0xB2 0x00 0x04 0x02 0x01 0x25 0x01 0xFF

5-2 Setting 12-1 : Line Adjustment

5-2-16 Line Adjustment 1

[Settings]

Command setting destination : ASIC (Example :0xA2 ALL ASIC)

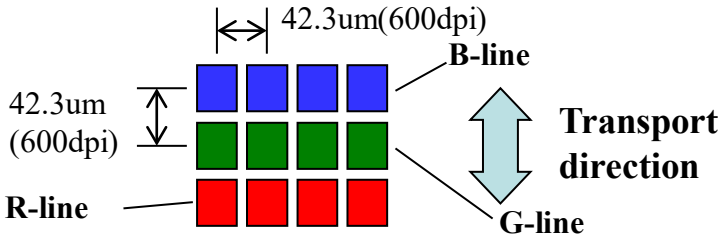
Address	Register Name	Function
0x03C7 (bit b2)	VMS _BYPASS	Select Line Adjustment ON / OFF (bit b2) "0" : Line Adjustment ON "1" : Line Adjustment OFF **※Please note that the settings are the opposite of the other register settings.**
0x03C7 (bit b0)	RBSEL	Select the transport direction (bit b0) "0": KDAX4 normal direction. (B → G → R : B-line first) "1": KDAX4 opposite direction. (R → G → B : R-line first)

[Register Map]

Must not change the "0" fixed bit.

	b7	b6	b5	b4	b3	b2	b1	b0
0x03C7						VMS _BYPASS	0	RBSEL

[Conceptual diagram of Line Adjustment]



Each RGB scanning line is offset by one pixel of 600dpi in the transport direction.

This function uses the built-in line memory to delay the other two lines (G line and B line) with respect to the R line, so that the image for each line is aligned with the same position on the medium (at the time of initial setting).

[Line Adjustment 1]

[Function] This function is to match the images of RGB pixels at different positions in the medium transport direction with the image of the medium at the same position.

[Initial Setting]

1. Line Adjustment ON **(VMS_BYPASS= 0)**
2. The transport direction
   KDAX4 normal direction. (B → G → R : B-line first)
   (RBSEL = 0)

[Setting mode]

1. Select the transport direction.
   ・KDAX4 normal direction. (B → G → R : B-line first)
   ・KDAX4 opposite direction. (R → G → B : R-line first)
2. Select Line Adjustment ON / OFF

[Notice]

(1) An unstable transportation speed may cause a color bleeding or blurring.
(2) Please refer to the next page as well and set.
(3) This function is not to completely control a color bleeding or blurring. Use the effect of this function after confirmation enough.
(4) When performing Line Adjustment on the user's system side, turn off this function and use the data.
(5) For details on settings, refer to the Function Specifications.

Example of Communication Command

Line Adjustment ON

(KDAX4 normal direction. (B → G → R : B-line first) **)**

0x1B 0xA2 0x00 0x04 0x02 0x03 0xC7 0x00 0xFF

Line Adjustment OFF

0x1B 0xA2 0x00 0x04 0x02 0x03 0xC7 0x04 0xFF

5-2 Setting 12-2 : Line Adjustment

5-2-17 Line Adjustment 2

[Settings]

Command setting destination : ASIC (Example :0xA2 ALL ASIC)

Address	Register Name	Function
0x03C2 0x03C3	RATIO	Resolution in transportation direction／600dpi Ratio. (Settable range from 0.03 to 4.0) Settable register range : 1(0001h) - 16384(4000h)
0x03C4 0x03C5	OFSET	Set the offset amount of the green pixel position (Internal division ratio of the movement range for the green pixel). Offset amount internal division ratio settable range : 0 - 4095 /4096 Settable register range : 0(0000h) - 4095(0FFFh)

[Register Map]

	b7	b6	b5	b4	b3	b2	b1	b0
0x03C2	RATIO(7:0)							
0x03C3		RATIO(14:8)						
0x03C4	OFSET(7:0)							
0x03C5					OFSET(11:8)			

[Pixel position adjust for Line Adjustment]

Use the RAITO and OFSET registers to adjust the RGB pixel position during Line Adjustment. Refer to the Function Specifications (TM-XL551) for the details of the settings.

[Line Adjustment 2]

[Function] Adjust the pixel position to match RGB pixels at different positions in the medium transport direction with the medium at the same position.

[Initial Setting]

1. Resolution in transportation direction / 600dpi(42.3µm) Ratio 1.0 (RATIO = 1000h)
2. The offset amount of the green pixel position 0 (Internal division ratio of the movement range for the green pixel 0) (OFSET = 0000h)

[Setting mode]

1. Resolution in transportation direction ／600dpi(42.3µm)

$$\text{RATIO} = \frac{\text{Register setting value (decimal number)}}{4096}$$

2. The offset amount of the green pixel position

$$\text{OFSET} = \frac{\text{Register setting value (decimal number)}}{4096}$$

[Notice]

(1) Please set according to the Line Adjustment 2 described on the previous page.

Example of Communication Command

RATIO 1.0

(Resolution in transportation direction ／600dpi(42.3µm))

0x1B 0xA2 0x00 0x05 0x02 0x03 0xC2 0x00 0x10 0xFF

By setting Parameter Size to 0x05
Writing to two consecutive addresses is possible.

OFSET(Internal division ratio of the movement range for the green pixel)

0x1B 0xA2 0x00 0x05 0x02 0x03 0xC4 0x00 0x00 0xFF

5-2 Setting 13 : γ Correction

5-2-18 γ Correction function

[Settings]

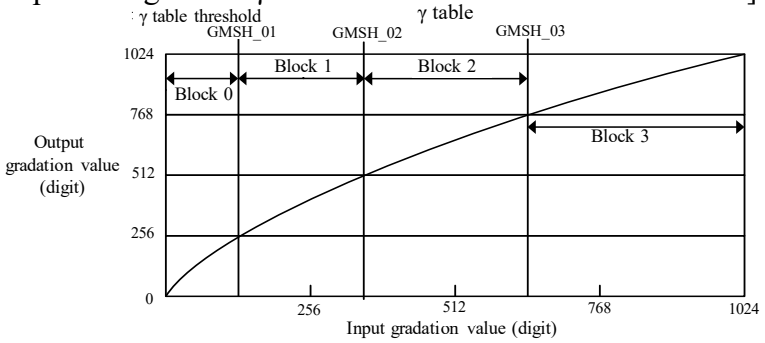
Command setting destination : FPGA (Example :0xB2 ALL FPGA)

Address	Register Name	Function
0x0160	GAMMA _ENB	Set γ Correction ON / OFF "0" : γ Correction OFF "1" : γ Correction ON

[Register Map]

	b7	b6	b5	b4	b3	b2	b1	b0
0x0160								GAMMA _ENB

[Conceptual diagram of γ Correction and data conversion table]



Data conversion correspondence table

Converted data	Block 0 0-128 gradation	Block 1 129-346 gradation	Block 2 347-640 gradation	Block 3 641-1023 gradation
9	0	0	1	1
8	0	1	0	1
7	8bit-SRAM 00h to FFh	8bit-SRAM 00h to FFh	8bit-SRAM 00h to FFh	8bit-SRAM 00h to FFh
6				
5				
4				
3				
2				
1				
0_LSB				

[γ Correction]

[Function]

Change the linearity of the image output.

[Initial Setting]

1. γ Correction OFF : γ = 1 (Linear) **(0x0160 = 00h)**
2. Correction coefficient setting :
   Setting example on the left (γ = 2.2)

[Setting mode]

γ Correction ON/OFF

[Notice]

(1) The γ correction function of this product divides 1024 steps (10bits length) into 4 blocks as shown in the figure on the left. The tone is specified by specifying 256 data (8bit length) in the Block using the data table.

(2) γ correction can be set for each color.

(3) Please contact us for changing the detailed settings of γ correction.

Example of Communication Command

γ correction ON : γ correction function ON

0x1B 0xB2 0x00 0x04 0x02 0x01 0x60 0x01 0xFF

γ correction OFF : γ correction function OFF

0x1B 0xB2 0x00 0x04 0x02 0x01 0x60 0x00 0xFF

5-2 Setting (others) : Test Pattern

5-2-19 Test Pattern

[Settings]

Command setting destination : ASIC (Example :0xA2 ALL ASIC)

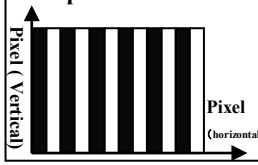
Address	Register Name	Function
0x0345 (bit b0)	PTNON	Set Test Pattern ON / OFF (bit b0) "0" : OFF (Normal Output)、 "1" : ON
0x0345 (bit b2,3,4)	PTNCOL	ON / OFF control for each R / G / B output of test pattern. "0":Test Pattern, "1": Data of specified color 0 mask.
0x0346 (bit b0,1)	PTNSEL1	Select Test pattern (arrangement of "bit b1" and "bit b0") "0" : Stripe of horizontal ,"1":Grey ramp horizontal "2" : Grey ramp vertical, "3" : RGBW
0x0346 (bit b2,3)	PTNSEL2	Select Test Pattern gradation. 1. For Stripe of horizontal. "0": 32 pixels width ,"1": 64 pixels width "2": 128 pixels width ,"3" : 256 pixels width 2. For Gray ramp horizontal "0": 1 gradation / pixel, "1": 2 gradations / pixel "2": 4gradations / pixel, "3": 8gradations / pixel 3. For Gray ramp vertical "0": 1 gradation / line, "1": 8 gradations / line "2": 16 gradations / line, "3": 32 gradations / line

[Register Map]

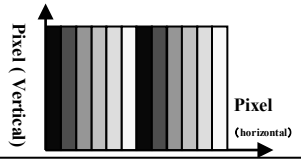
	b7	b6	b5	b4	b3	b2	b1	b0
0x0345				TPCOL(2:0)				TPON
0x0346					TPSEL2(2:0)		TPSEL1(2:0)	

[Conceptual diagram of an image example of Test Pattern]

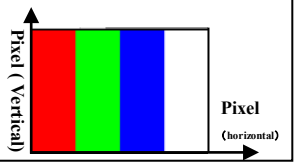
<Stripe of horizontal>



<Gray ramp horizontal>



<RGBW>



[Output of Test Pattern]

[Function]

Outputs the Test Pattern image used to check the connection between this product and the user-side system.

[Initial Setting]

1. Test Pattern OFF **(0x0345 = 00h)**
   (Output the image scanned from the sensor IC)
2. Select Test Pattern : Stripe of horizontal, 32 pixels width **(0x0346 = 00h)**

[Setting mode]

1. Output Test Pattern / Normal mode (scanned image output)
   (Test pattern set at the time of shipment from the factory)

[Notice]

(1) Image data transfer is a function for checking the connection between this product and the user system.

(2) When the Test Pattern is output, the scanned image is not output.

(3) When using, turn off Dark Correction, White Correction, and γ Correction.

Example of Communication Command

Test Pattern ON

0x1B 0xA2 0x00 0x04 0x02 0x03 0x45 0x01 0xFF

Test Pattern OFF (Output Normal image)

0x1B 0xA2 0x00 0x04 0x02 0x03 0x45 0x00 0xFF

Checking the ASIC1 Test Pattern (Read)

0x1B 0x11 0x00 0x04 0x03 0x03 0x45 0xFF

5-2 Setting (Others) : Software Boot 1

5-2-20 Description of Software Boot function

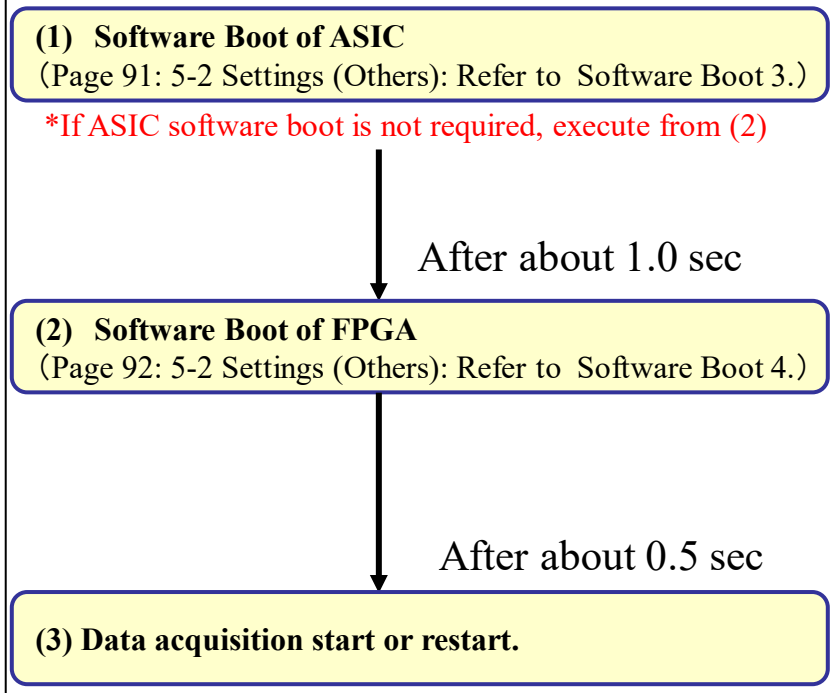
This product is equipped with a function (software boot function) that can be reset from the EEPROM by resetting by register setting.

Software boot is an independent FPGA and ASIC. Please do it for FPGA or ASIC individually or collectively.
For the operation method, refer to page 91: 5-2 Settings (others): Software boot 3 and page 92: 5-2 Settings (others): Software boot 4.

The functions that are reset by software boot are listed for each function, so please refer to them and use the reset function.
(Page 90: 5-2 Settings (Others): See Software Boot 2)

When Software Booting, it will take some time as it will read all the data from the EEPROM. Therefore, it is recommended to wait 1.0 seconds for ASIC and 0.5 seconds for FPGA before executing each software boot and data acquisition after software boot.
Also, please do not enter the command on the way. (The value of the register may be overwritten, and the data in the EEPROM may be overwritten.)

[Recommended flow overview]



5-2 Setting (Others) : Software Boot 2

5-2-20 Software boot correspondence table

The following is a list of the functions that are initialized by the data in the EEPROM for each Software Boot of FPGA and ASIC.

Explanatory note :

○ : Registers initialized to the data in EEPROM by software boot.

× : Registers that is not initialized to the data in EEPROM by software boot.

Item	Functions corresponding to software boot	
	ASIC	FPGA
— Set UART Baud Rate	×	×
— Set the time until communication reset when a communication error occurs.	×	○
1. Output Camera Link™ Clock Frequency	×	○
2. Output Camera Link™ Configuration	×	○
3. Resolution Selecting	×	○
4. Line Sync Input	×	○
5. Output Width Setting	×	○
6. Dark Correction	○	×
7. LED Illuminations Control and Setting	○	×
8. White Correction	○	×
9. PGA	○	×
10. Interpolation	×	○
11. Overlap Output	×	○
12. Line Adjustment	○	×
13. γ Correction	×	○

[Caution]

(1) Software boot controls the Status Register of each FPGA and ASIC. Unlike normal register control commands, Status Register does not specify a register address, so refer to the communication command example carefully and execute it. (Even if the setting is wrong, it will not be broken.)

(2) When rebooting, the setting value is read from EEPROM.

(3) Software booting of ASIC and FPGA data can be performed individually, and even if they are performed individually, there is no problem in terms of function and no communication error occurs.

As this product specification, it is recommended to perform FPGA software boot after ASIC software boot.

(4) If there is an error in the image output after software booting only the ASIC, please perform software booting of the FPGA or turning on the power again to return it to the factory default state.

(5) The UART communication baud rate is not initialized by either ASIC or FPGA software boot.

Software Boot is maintained at the setting value before applying the software reset. The UART communication Baud Rate setting is initialized only by turning on the power supply again.

5-2 Setting (Others) : Software Boot 3

5-2-21 ASIC Software Boot

[Settings]

Command setting destination : ASIC (Example :0xA4 ALL ASIC)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	BANK(1)	BANK(0)	BTST	XBOOT

Register Name	R/W	Function
XBOOT	R	Boot Status : ”0” During Boot. , ”1” Boot Complete.
BTST	R/W	Soft reset trigger signal. Boot start with transition from “0” to “1”
BANK(1:0)	R/W	Specify the memory bank number of the access destination. "00": ASIC register (Normally, select "00") “01”: Dark Correction coefficient “10”: White Correction coefficient

* Since the above setting has a Register with only the read function of “R”, the R / W column is set.

[ASIC Software Boot]

Example of Communication Command

0x1B 0xA4 0x00 0x02 **0x01** 0x00 0xFF

0x1B 0xA4 0x00 0x02 **0x01** 0x02 0xFF

Status Register Write

* Please send the above two commands in succession.

[Check boot status]

Example of Communication Command

Read ASIC-1 status register

0x1B 0x13 0x00 0x02 **0x05** 0xFF

Status Register Read

* Confirm that XBOOT transitions to "1".
* If you can’t confirm XBOOT transition, please prepare a timeout function on the system side.

[ASIC Software Boot function]

[Function]

Rewrite the operating parameters of the CIS built-in ASIC with the contents of the EEPROM connected to the ASIC.

Performing a software reset initializes all of the BANK (1: 0) ASIC registers, Dark Correction coefficient, and White Correction coefficient.

[Initial Setting]

—

[Setting mode]

—

[Notice]

(1) All register values are rewritten to the initial values (the contents of the EEPROM connected to the ASIC).
If you change the operation mode of CIS and use it, one of the following is required.
1. Write the control parameters at the time of CIS startup to the EEPROM connected to the ASIC.
2. After booting the software, perform the settings again after starting the power supply.

(2) It takes 1.0 sec for all registers to be rewritten after Software Boot.

[Checking the status register]

The internal operating status of CIS (same for both hardware and software boot) can be checked by reading the register XBOOT.

[Notice]

(1) Specify each ASIC and read it.
(2) Since it is necessary to check the FPGA / ASIC when reading the Status Register, set the SELBUS signal to "0".

5-2 Setting (Others) : Software Boot 4

5-2-22 FPGA Software Boot

[Settings]

Command setting destination : FPGA (Example :0xB4 ALL FPGA)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	BTST	XBOOT

Register Name	R/W	Function
XBOOT	R	Boot Status : ”0” During Boot. , ”1” Boot Complete.
BTST	R/W	Soft reset trigger signal. Boot start with transition from “0” to “1”

* Since the above setting has a Register with only the read function of “R”, the R / W column is set.

[FPGA Software Boot]

Example of Communication Command

0x1B 0xB4 0x00 0x02 **0x01** 0x00 0xFF

0x1B 0xB4 0x00 0x02 **0x01** 0x02 0xFF

Status Register Write

* Please send the above two commands in succession.

[Check boot status]

Example of Communication Command

Read FPGA-1 status register

0x1B 0x73 0x00 0x02 **0x05** 0xFF

Status Register Read

* Confirm that XBOOT transitions to "1".
* If you can’t confirm XBOOT transition, please prepare a timeout function on the system side.

[FPGA Software Boot function]

[Function]

Rewrite the operating parameters of the FPGA built into the CIS with the contents of the EEPROM connected to the FPGA.

[Initial Setting]

—

[Setting mode]

—

[Notice]

(1) All register values are rewritten to the initial values (the contents of the EEPROM connected to the FPGA). If you change the operation mode of CIS and use it, one of the following is required.
1. Write the control parameters at the time of CIS startup to the EEPROM connected to the ASIC.
2. After booting the software, perform the settings again after starting the power supply.

(2) It takes 0.5 sec for all registers to be rewritten after Software Boot.

(3) Please note that the Baud Rate is not initialized, and the set value is maintained.

[Checking the status register]

The internal operating status of CIS (same for both hardware and software boot) can be checked by reading the register XBOOT.

[Notice]

(1) Specify each FPGA and read it.

(2) Since it is necessary to check the FPGA / ASIC when reading the Status Register, set the SELBUS signal to "0".

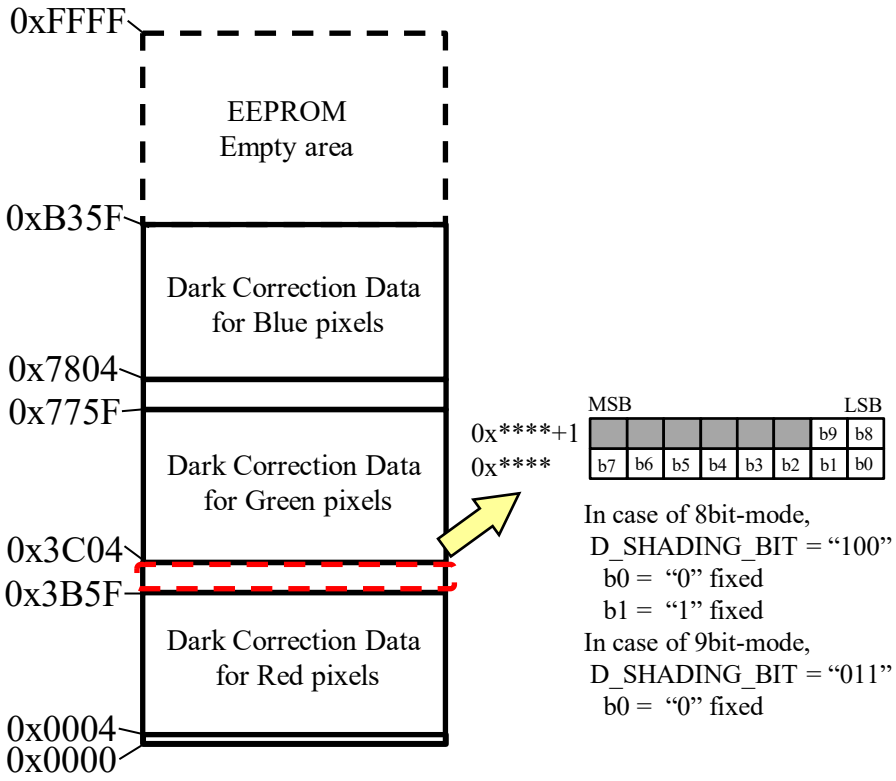
Appendix A: Application notes

[Appendix A-1: Dark and White Correction value allocation]

KD-CIS AX4 Dark and White Correction memory mapping
（KD-CIS AX4 Dark/White Correction Data – Memory Mapping）

Dark Correction data

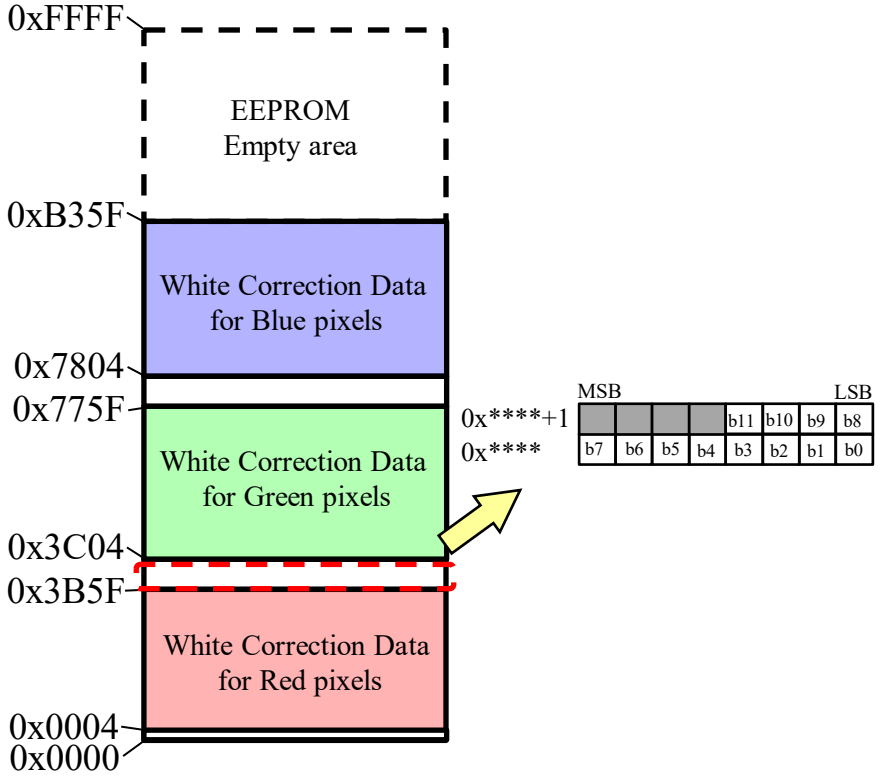
Dark correction data has 10bit width and occupy 2 address.



In case of 8bit-mode,
D_SHADING_BIT = “100”
b0 = “0” fixed
b1 = “1” fixed
In case of 9bit-mode,
D_SHADING_BIT = “011”
b0 = “0” fixed

White correction data

White correction data has 10bit width and occupy 2 address.



Appendix A: Application notes

[Appendix A-2 : List of Frame Grabber and operation check]

Frame Grabber maker	Type	Operation Check	Camera files can be provided
Matrox	SOL 2M EV CLB	○	○
	RAD EV 1G CLSF/CLDF	○	○
AVAL DATA			
BitFlow Inc			
LINX			
TELEDYNE DALSA			
National Instruments			
Silicon Software			
Cognex			

Appendix A: Application notes

(Note) The following lists only the registers listed in this document.
Please refer to the Function Specifications (TM-XL551) for more detailed functions.

[Appendix A-3 : Register List]

1. Command (Setting destination) : **0xB2 (ALL FPGA)**

[Register address for setting to FPGA]

Address	Register name	R/W	Setting value	Function	Initial Setting
0x0116	TIMEOUT	R/W	0 to 255	Communication reset ON / OFF and time set **"0" (00h) Invalid** - (No reset when communication error occurs) **"1" (01h) valid** - In case of communication error, this product will reset in 0.2 sec. **"2"～"255" (02h～FFh) Valid** - The time until the reset is extended by the set value ((decimal number) x 0.2 sec).	1
0x0118	OCLK_SEL	R/W	0 to 28	Set Camera Link™ Clock Frequency "0"(00h) 48MHz to "28"(1Ch) 84MHz To select the Camera Link ™ output clock frequency, refer to the frequency correspondence table P.72 .	28
0x0120	DATA_FORM	R/W	0 to 3	Camera Link ™ output format switching "0" (00h) (Type B-1) 24bit-RGB No.1 (Base Configuration) "1" (01h) (Type B-2) 24bit-RGB No.2 (Base Configuration × 2) "2" (02h) (Type A) 24bit-RGB x 2(Medium Configuration) "3" (03h) (Type C) 30bit-RGB (Medium Configuration)	0
0x0123	EXTRA_PIXEL	R/W	0 to 1	Set pixel overlap ON / OFF "0" (00h) Overlap OFF "1" (01h) Overlap ON	0
0x0124	RESOLUTION	R/W	0 to 3	Select the resolution of the output images. "0"(00h) 600dpi , "1"(01h) 300dpi "2"(02h) 200dpi , "3"(03h) 150dpi	0
0x0125	EX_PIXNUM	R/W	0 to 1	Select the number of overlap pixels. "0"(00h) : Overlap pixels 22pixels "1"(01h) : Overlap pixels 84pixels	0

Appendix A: Application notes

[Appendix A-3 : Register List]

(Note) The following lists only the registers listed in this document.
Please refer to the Function Specifications (TM-XL551) for more detailed functions.

1. Command (Setting destination) : **0xB2 (ALL FPGA)**

[Register address for setting to FPGA]

Address	Register name	R/W	Setting value	Function	Initial Setting
0x0126 0x0127	OUT_XOFFSET	R/W	0 to 65535	Offsets the output start position of the sensor pixels. The output start position is offset by the set value.	0
0x0128 0x0129	OUT_WIDTH	R/W	0 to 65535	Set the number of valid output pixels from the pixels set by OUT_XOFFSET.	A1/A0/A3 7296 A3+ 7904
0x0132	PIX_INTERP_ENB	R/W	0 to 1	Set the interpolation ON / OFF. “0”(00h) Interpolation OFF “1”(01h) Interpolation ON	0
0x0160	GAMMA_ENB	R/W	0 to 1	Set γ Correction ON / OFF “0” : γ Correction OFF “1” : γ Correction ON	0
0x01A0	EXTSYNC	R/W	0 to 1	Select sync. mode “0”(00h) Internal Sync mode “1”(01h) External Sync mode	1
0x01A1 0x01A2	H_CYCLE	R/W	0 to 65535	Line cycle setting in internal sync Mode. $\text{Setting line cycle}(\mu\text{sec}) = \frac{(\text{Register setting value} + 1)}{\text{Camera Link™ Frequency (MHz)}}$	65535
0x3390	UCOMSEL	R/W	0 to 1	Communication mode “0”: AX4 original “1”: AX3 compatibility mode	0
0x4001	BAUD_RATE	R/W	0 to 3	Select Baud Rate “0” (00h) 9.6kbps , “1” (01h) 19.2kbps “2” (02h) 115.2kpbs , “3” (03h) 19.2kbps	3

Appendix A: Application notes

(Note) **The following lists only the registers listed in this document.**
Please refer to the Function Specifications (TM-XL551) for more detailed functions.

[Appendix A-3 : Register List]

1. Command (Setting destination) : **0xA2 (ALL ASIC)**

[Register address for setting to ASIC]

Address	Register name	R/W	Setting value	Function	Initial Setting
0x030A (bit b3～b0)	MAX-HOLD	R/W	0 ,2,15	Max.Hold mode White Correction data generation trigger (corresponding to bit b3 to b0). Trigger on at the transition from “2” (0010b) to "0" (0000b) (when bit b4 = 1) *Please change from “15”(1111b) to "2" (0010b) in advance.	15
0x030C	LED_CONT_ENB	R/W	0, 4, 8, 12	Select illumination mode “0” (00h) Illumination OFF. “4” (04h) One side illumination(B) ON. Lower-stream side illumination(B) ON. “8” (08h) One side illumination(A) ON. Upper-stream side illumination(A) ON. “12” (0Ch) Both side illuminations ON. Upper-stream side illumination(A) and Lower-stream side illumination(B) ON.	12
0x030D 0x030E	LEDS0	R/W	0 to 65535	Set illumination lighting start position. (Do not change this register from the initial value because it matches the image scanning timing of the sensor IC.) Initial value 34 (0022h)	34
0x030F 0x0310	LED0W0	R/W	0 to 65535	Lower-stream side illumination(B) period setting. Example) In the case of 37.5 µs, common to illumination (A) and (B) 37.5 µs / 29.15 ns ≒ 1287 (Decimal number, rounded up) Hexadecimal conversion 0x030F 07h, 0x0310 05h	1287
0x0311 0x0312	LED1W0	R/W	0 to 65535	Upper-stream side illumination(A) period setting. The example is the same as the above "LED0W0"	1287
0x0313 0x0314	LEDT0	R/W	0 to 65535	Set illuminations effective period. Initial value 63353(FFFFh)	65535
0x032D	LEDN0	R/W	0 to 4	Set illumination Pulse division. “0”(00h) OFF , “1”(01h) 2pulse , “2”(02h) 4pulse , “3”(03h) 8pulse ”4”(04h) 16pulse	0

Appendix A: Application notes

[Appendix A-3 : Register List]

(Note) The following lists only the registers listed in this document.
Please refer to the Function Specifications (TM-XL551) for more detailed functions.

1. Command (Setting destination) : **0xA2 (ALL ASIC)**
   [Register address for setting to ASIC]

Address	Register name	R/W	Setting value	Function	Initial Setting
0x0342 (Bit b0)	D_SHADING_SET	R/W	0 to 1	Automatic generate Dark Correction Data. Generated trigger ON by “0” → "1“. (Notice) Don’t change the value of other bits of 0x0342.	0
0x0342 (Bit b1)	W_SHADING_SET	R/W	0 to 1	Normal mode White correction data generation trigger (bit b1). Trigger ON by transition “0” → "1“. (Notice) Don’t change the value of other bits of 0x0342.	0
0x0342 (Bit b2)	W_COL_MODE	R/W	0 to 1	Select the White Correction mode. (corresponding to bit b3) (Notice) Don’t change the value of other bits of 0x0342.	0
0x0375	R/G/B_DARK_ENB	R/W	0 to 7	Dark Correction ON / OFF control for each color of R / G / B “0” OFF, “1” ON bit0 : B_DARK_ENB ON/OFF Control bit1 : G_DARK_ENB ON/OFF Control bit2 : R_DARK_ENB ON/OFF Control	0
0x0396	R/G/B_ WHITE_ENB	R/W	0 to 7	When W_COL_MODE = “0” (see next page). White Correction ON / OFF control for each color of R / G / B. b2-R, b1-G, b0-B each signal "0" OFF, "1" ON bit0 : B_WHITE_ENB ON/OFF Control bit1 : G_WHITE_ENB ON/OFF Control bit2 : R_WHITE_ENB ON/OFF Control	0
0x03B2	R/G/B_ SBSHFF	R/W	0 to 7	When W_COL_MODE = “1” (see next page). White Correction ON / OFF control for each color of R / G / B. b2-R, b1-G, b0-B each signal "0" OFF, "1" ON bit0 : B_SBSHFF ON/OFF Control bit1 : G_SBSHFF ON/OFF Control bit2 : R_SBSHFF ON/OFF Control	0

Appendix A: Application notes

[Appendix A-3 : Register List]

(Note) The following lists only the registers listed in this document.
Please refer to the Function Specifications (TM-XL551) for more detailed functions.

1. Command (Setting destination) : **0xA2 (ALL ASIC)**

[Register address for setting to ASIC]

Address	Register name	R/W	Setting value	Function	Initial Setting
0x037C	PGA_SW	R/W	0 to 1	Set PGA gain ON/OFF. “0”(00h) PGA(gain)OFF “1”(01h) PGA(gain)ON	0
0x037D 0x037E	REG_R	R/W	-1024 to 3071	Set the value of Red PGA. The calculation is based on the right formula. Set the sign with b4 of 0x037E. “0”:+, “1”: - Settable range From -1024 (1400h) to 3071 (0BFFh). $\text{PGA Output Data} = \frac{1024 + \text{Register value (Decimal Number)}}{1024} \times \text{Input data}$	0
0x037F 0x0380	REG_G	R/W	-1024 to 3071	Set the value of Green PGA. The calculation is based on the right formula. Set the sign with b4 of 0x0380. “0”:+, “1”: - Settable range From -1024 (1400h) to 3071 (0BFFh).	0
0x0381 0x0382	REG_B	R/W	-1024 to 3071	Set the value of Blue PGA. The calculation is based on the right formula. Set the sign with b4 of 0x0382. “0”:+, “1”: - Settable range From -1024 (1400h) to 3071 (0BFFh).	0
0x0398 0x0399	R_WHITE_TARGET	R/W	0 to 4095	Set the R White Correction Target value. Setting range: 0-4095, **Initial value: 4000.**	4000
0x039A 0x039B	G_WHITE_TARGET	R/W	0 to 4095	Set the G White Correction Target value. Setting range: 0-4095, **Initial value: 4000.**	4000
0x039C 0x039D	B_WHITE_TARGET	R/W	0 to 4095	Set the B White Correction Target value. Setting range: 0-4095, **Initial value: 4000.**	4000

Appendix A: Application notes

[Appendix A-3 : Register List]

(Note) The following lists only the registers listed in this document.
Please refer to the Function Specifications (TM-XL551) for more detailed functions.

1. Command (Setting destination) : **0xA2 (ALL ASIC)**

[Register address for setting to ASIC]

Address	Register name	R/W	Setting value	Function	Initial Setting
0x03C2 0x03C3	RATIO	R/W	1 to 16384	Resolution in transportation direction／600dpi Ratio. (Settable range from 0.03 to 4.0) Settable register range : 1(0001h) - 16384(4000h) $\text{RATIO} = \frac{\text{Register setting value (decimal number)}}{4096}$	4096
0x03C4 0x03C5	OFSET	R/W	0 to 4095	Set the offset amount of the green pixel position (Internal division ratio of the movement range for the green pixel). Offset amount internal division ratio settable range : 0 - 4095 /4096 $\text{OFSET} = \frac{\text{Register setting value (decimal number)}}{4096}$	0
0x03C7 (bit b2)	VMS_BYPASS	R/W	0 to 1	Select Line Adjustment ON / OFF (bit b2) “0” : Line Adjustment ON “1” : Line Adjustment OFF **※Please note that the settings are the opposite of the other register settings.**	0
0x03C7 (bit b0)	RBSEL	R/W	0 to 1	Select the transport direction (bit b0) “0”: KDAX4 normal direction. （B → G → R : B-line first) “1”: KDAX4 opposite direction.（R → G → B : R-line first)	0

Appendix A: Application notes

[Appendix A-3 : Register List]

(Note) The following lists only the registers listed in this document.
Please refer to the Function Specifications (TM-XL551) for more detailed functions.

1. Command (Setting destination) : **0xA2 (ALL ASIC)**

[Register address for setting to ASIC]

Address	Register name	R/W	Setting value	Function	Initial Setting
0x0345 (bit b0)	PTNON	R/W	0 to 1	Set Test Pattern ON / OFF (bit b0) “0”:OFF(Normal Output), “1”:ON	0
0x0345 (bit b1)	PTINV	R/W	0 to 1	Test Pattern inversion control (bit b1) “0”:OFF(Normal Output), “1”:ON(Inversion)	0
0x0345 (bit b2,3,4)	PTCOL	R/W	Each bit 0 to 1	ON / OFF control for each R / G / B output of Test Pattern. “0”:Test Pattern, ”1”: Data of specified color 0 mask. b2 : R data 0 Mask ON/OFF Control b3 : G data 0 Mask ON/OFF Control b4 : B data 0 Mask ON/OFF Control	0
0x0346 (bit b0,1)	PTNSEL1	R/W	0 to 3	Select Test pattern (arrangement of "bit b1" and "bit b0") “0”:Stripe of horizontal ,”1”:Grey ramp horizontal “2”:Grey ramp vertical , ”3”:RGBW	0
0x0346 (bit b2,3)	PTNSEL2	R/W	0 to 3	Select Test Pattern gradation. 1. For Stripe of horizontal. “0”: 32 pixels width ,”1”: 64 pixels width “2”: 128 pixels width ,”3”: 256 pixels width 2. For Gray ramp horizontal “0”: 1 gradation / pixel, ”1”: 2 gradations / pixel “2”: 4gradations / pixel, ”3”: 8 gradations / pixel 3. For Gray ramp vertical “0”: 1 gradation / line, ”1”: 8 gradations / line “2”: 16 gradations / line, ”3”: 32 gradations / line	0

Appendix B: Q & A

1. Questions about operating environment

No.	Topic	Question	Answer
1	Peripherals	Do you rent a PC in which frame grabber is installed?	No. Please ask frame grabber manufactures. Some of them rental Frame Grabbers.
2	SDK	Is there SDK exclusive for KD-CIS?	No, there isn't.
3	Frame grabber	Which frame grabber can I use?	See Appendix A-2.
4	Frame grabber	What kind an interface specification do I need for PC ?	Check the operating environment of your Frame Grabber.

2. Questions about specifications

No.	Topic	Question	Answer
1	Standards	Does KD-CIS meet CE standards?	KD6R309AX4, KD6R335AX4, KD6R617AX4, KD6R309AX4-NL, KD6R617AX4-NL are CE marking Compliant. (Other models are not compliant.) CE marking compliant products have a CE Label.
2	Standards	Does KD-CIS meet eye-safe standard of IEC62471/EN62470?	Design wise, there is no problem against eye-safe. But we haven't taken an official certification of IEC62471/EN62470.
3	Standards	Does KD-CIS meet RoHS and REACH?	Yes, it does.
4	Control method	Can I synchronize several KD-CISs?	There is no function in CIS that enable synchronize several KD-CISs. 2pcs of 309mm size electric circuit units are synchronized in 617mm size KD-CIS and 3pcs of them are in 926mm size.
5	Control method	Can I control KD-CIS with external synchronization mode?	KD-CIS can be controlled using an external sync signal. For details, refer to the Data Sheet and Section 5-2 Setting 4 "Line Sync input".

Appendix B: Q & A

No.	Topic	Question	Answer
6	Control method	Can I store correction data ?	The correction data can be stored in the CIS and read out. For details, see the Function Specification TM-XL551.
7	Control method	Can you supply the camera files?	Please refer to Appendix A-2 for the camera files that can be provided.
8	Control method	Can I control exposure time of sensor by external signal?	This product determines the exposure time based on the light emission time of the illumination, and the sensor itself does not have exposure control (global shutter function).
9	Control method	Where can I find communication spec and detailed information about serial communication（Baud rate, command list etc…)	Refer to 4-4 Communication control.
10	Control method	Do I get error message when communication errors happen?	There is no communication error status. If an error occurs, it will automatically recover. The automatic recovery period can be set in the register.
11	Control method	What is a command for write white and dark correction data to EEPROM?	Please refer to the Function Specifications TM-XL551. (Supplementary material: Access to EEPROM).
12	Control method	What command should I use for write the correction data which is generated and stored in PC by me?	Please refer to the Function Specifications TM-XL551. (Supplementary material: Access to EEPROM).
13	Data communication	Can I use Baud Rate 9.6Kbps of camera link™ serial communication setting?	Baud Rate supports 9.6kbps, 19.2Kbps, 115.2Kbps.
14	Scanning speed	Can I increase line scan frequency by choosing lower resolution?	The Line rate can be increased by the scanning resolution. Please refer to the Data Sheet (TM-XL499) for details.
15	Power supply	Can you unify DC 24V for DC 5V and DC24V power supply?	This Product doesn't support it. (We are considering support for next-generation products).
16	Power supply	Why are there procedures about power ON/OFF?	If 24V is applied before 5V, LED-Duty control will not be performed (LED may light up at 100% duty). Therefore, if only 24V is applied for a long time, the product temperature may rise due to heat generated from the light source, and the product may deteriorate. In order to use the product for a long time, it is recommended that you follow the description in Section 4-8 "Recommended sequence for turning on and off the power supply".
17	Power supply	How GND of DC 5V and DC 24V are connected?	5V and 24V GND are shared in the board (light source lighting board).

Appendix B: Q & A

No.	Topic	Question	Answer
18	Resolution	Is this Possible to switch the resolution?	There is a resolution switching function (600, 300, 200, 150 dpi) using a simple average. Please refer to Section 5-2 Setting 3 “Resolution Selecting”.
19	Imaging System	What is a DOF(Depth of Focus) of KD-CIS?	Refer to Section 2-3 “Definition”.
20	Lenz	What is a diameter of the lens?	Φ = 1.049mm
21	Correction	Does KD-CIS have a function to adjust position of each RGB lines?	For the color shift correction function, refer to Section 5-2 Setting 12 "Line Adjustment".
22	Correction	Can I start White Correction by trigger signal?	No. But we are considering to apply it from next product.
23	Correction	Does KD-CIS have a function to adjust a distorted image?	There is no distortion correction function, but CIS can acquire images with small distortion in principle. The lenses mounted on the CIS are rod lenses (GRIN lenses) with a diameter of 1 mm arranged in an array. A rod lens is a lens that is imaged at the same magnification upright, that is, with 1: 1 dimensions without inversion of the subject. By arranging and using this lens in an array, the reading information is imaged on the reading system (photodiode array) while preserving the medium position. Since the optical system with such a configuration is used, the distortion of the lens is also local and small, and the reading position of each pixel as CIS is the same as the corresponding position of the medium. From the above, since there is almost no image distortion in the main scan (longitudinal direction of CIS), this product is not equipped with a distortion correction function.
24	Register setting	Can I store my own resister setting in the CIS besides Mitsubishi’s setting?	This Product does not support it. Please follow the steps below to set each time. ・ Save the initial value (factory default value) ・ Rewrite it in EEPROM. Please note that it is the customer's responsibility to rewrite it. For details, refer to the Function Specification TM-XL551.
25	Sensor IC	What is spectral sensitivity of KDAX4 Series?	Refer to 2-4 “Features of scanning pixels”.

Appendix B: Q & A

No.	Topic	Question	Answer
26	Illuminations	Can I get the LED setting document ?	Refer to the Function Specification TM-XL551.
27	Illuminations	Can I choose other LED? I would like to use IR light.	Illuminations of KDAX4 is white LED only. We recommend to use a non-illumination KDAX4 for whom requested LED with different wavelength.
28	Illuminations	What is spectrum of KDAX4?	Refer to 2-4 “Features of scanning pixels”.
29	Illuminations	Currently, there are two diffused reflection LEDs, but is it possible to add them? Also, if it can be added, can the illuminance adjustment be adjusted with the built-in CIS? (Including additional parts)	At present, there are no plans to develop extended light sources other than the standard light source. Please use a combination of a non-illumination type and an external light source prepared by the customer.
30	Illuminations	Is the initial state fully lit (LED-Duty = 100%)?	It is not fully lit. Illumination with the factory-setting duty value.
31	Operation	Is it okay to insert an external trigger when operating in the internal synchronization mode?	You can use it without any problem.
32	Dustproof and waterproof	Which IP level does KD-CIS fulfill?	We didn’t take IP test with our KDAX4. The module part which includes sensor ICs and SLA lens satisfies under JIS standard. JIS D 0207 (General rules of dust test for automobile parts) Test type F level 1 is cleared Dust type: JIS Z 8901(Loamy layer of Kanto district type 8) Dust density: 60,000[mg/m2] 1cycle is 10min interval after 5sec in the dust Total number of cycles :144cycle
33	Temperature	Where can I find caution regarding to temperature?	Refer to Section 2-7 “Specifications”. Please use it at a housing temperature of Tw = 70 degree or less.

Appendix C: AX4 Series Electronic Serial Label

[KDAX4 Serial Label storage register]

The following label information is stored.

Label information storage register: EEPROM of master FPGA (FPGA1)
(It is loaded into the FPGA at CIS boot. Setting destination: Command 0x71 FPGA1 Register Read)
Address : 0x0200 - 0x0204（5 Bytes）
Read address order and contents : See below. (BCD code)
* Please refer to the next page for the correspondence table between model numbers and models.

【 Example of Electric Serial Label 】

Serial No: 2112390001
CIS_Serial(0) : 0x0200 01h Last 4 digits of product serial (0001)
CIS_Serial(1) : 0x0201 00h
CIS_Serial(2) : 0x0202: 39h Model No. (KD6R309AX4)
CIS_Serial(3) : 0x0203: 12h Production month. (12 : December)
CIS_Serial(4) : 0x0204: 21h Production year. (2021)

Register Map（bit0:LSB）

Address	b7	B6	b5	b4	b3	b2	b1	b0
0x0200	CIS_SERIAL(0)							
0x0201	CIS_SERIAL(1)							
0x0202	CIS_SERIAL(2)							
0x0203	CIS_SERIAL(3)							
0x0204	CIS_SERIAL(4)							

Appendix C: AX4 Series Electronic Serial Label

[Label information read command]

0x1B 0x71 0x00 0x08 0x03 0x02 0x00 0xFF
FPGA1 register read : 5 bytes from Address 0x0200

(Read example)
0x01 0x00 0x39 0x12 0x21
KD6R309AX4 0001st product produced in December 2021.

[List of correspondence between model No. and model]

Model No.	Model Name	Model No.	Model Name
39	KD6R309AX4	45	KD6R335AX4
40	KD6R617AX4		
41	KD6R926AX4		
42	KD6R309AX4-NL		
43	KD6R617AX4-NL		
44	KD6R926AX4-NL		

Appendix D : Illumination Control architecture

[KDAX4 series LED illumination control concept of lighting period adjustment]

(Refer to the next page)

(Basic architecture)

(1) Determining the non-illumination period and maximum lighting period of the illumination for the reading period

・Used register　Setting non-lighting period : LEDS0 (Register Address 0x030D / 0x030E)

Maximum lighting period : LEDT0 (Register Address 0x0313 / 0x0314)

(Precautions)

1. Based on this period even if the scanning cycle from the External Sync, the range of the lighting period is determined.
2. The setting of the illumination period that exceeds the maximum lighting period is invalid, and the light is forcibly turned off during the maximum lighting period.

(2) Determining the illumination period

・Used Register　Lighting period of A side illumination : LED1W0 (Register Address 0x0311 / 0x0312)

Lighting period of A side illumination : LED0W0 (Register Address 0x030F / 0x0310)

(Precautions)

1. Determines any lighting period up to the maximum lighting period.
2. By default, the illumination period is set to approximately 85% (37.5 µsec / Line) at the minimum scanning cycle (44 µsec / Line) at A3 size 600 dpi.

(3) Determine illumination Pulse division.

・Used Register　Number of divisions setting : LEDN0 (Register Address 0x032D)

(Precautions)

1. The divided lighting of the illumination is lit according to the timing when the maximum lighting time set in item (1) is equally divided, and the individual lighting period is the period in which the lighting period set in item (2) is divided.
2. Determine the number of divisions according to the reading cycle per line, which is calculated from the line frequency during actual use. If you have a long line period and you want to distribute the illumination over the entire line period width, it is recommended to divide the illumination period.
3. Since there is an ON / OFF time for the lighting when the lighting is divided and turned on, the illuminance is lower than when the lighting is not divided.
   Please adjust the lighting period according to the number of divisions.

Appendix D : Illumination Control architecture

[Characteristics during Illumination control]

The figure of the measurement data is shown below.
The following measurement waveforms are shown in the data diagram.

- LED cont. : Control signal for illuminations.
- LED current : Current supplied to the LED
- LED illuminance : LED emission intensity

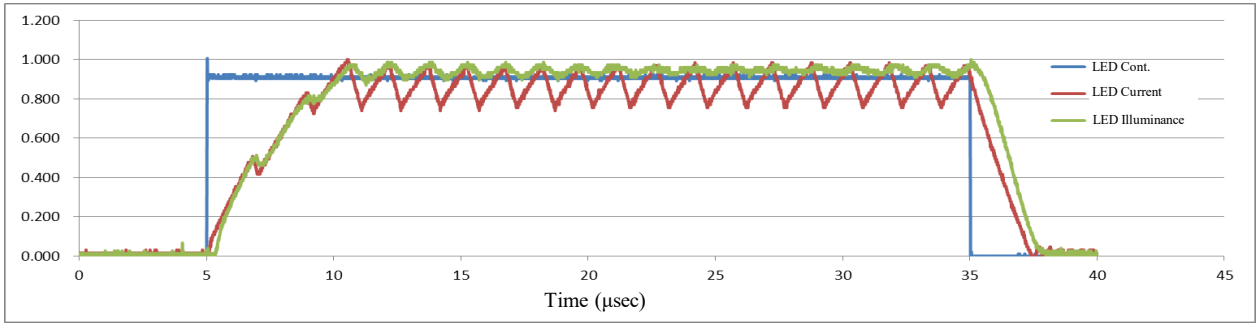


Fig. 1 Overall waveform of LED illumination emission.

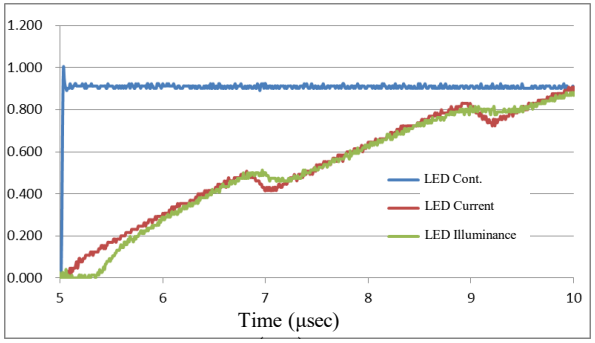


Fig. 2 Waveform at the start of LED illumination.

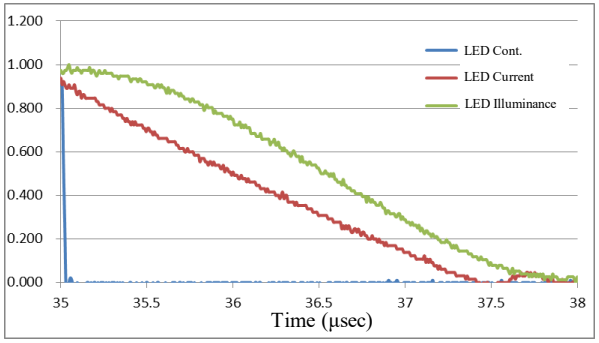


Fig. 3 Waveform when LED is OFF

Appendix D : Illumination Control architecture

[Illumination on / off characteristics]

1. Estimating the amount of delay when the illumination is on

From Fig. 2 on the previous page, the LED emission is delayed with respect to the LED control switch waveform. The delay until 100% lighting is about 5µsec, and the integrated light emission during this period is about 55%. (Ratio when 100% lighting is continued for 5µsec.)

Therefore, the amount of delay as seen from the illumination level is 5µsec x 0.45 = 2.75µsec.

2. Delay when illumination is OFF

From Fig. 3, it takes about 3µsec for the LED control waveform to turn off completely.

The illuminance during this 3µsec period is approximately 54% when the LED lights 100% for the delay time. Therefore, the delay time when the LED is turned off is 3µsec x 0.54 = 1.62µsec.

From the above results, the light source emission time of the CIS is apparently compared to the value set in the register.

1.13µsec (= 2.75－1.62) Light emission pulse width is narrow.

This value is generated for each pulse control, so if the illumination is performed with multiple pulses, the emission time can be reduced by the number of pulses Will occur.

For example, when split lighting control of 4 pulses is performed, the illuminance will be smaller by 4 × 1.13µsec = 4.52µsec than when short pulses are set.

In addition, when dividing illumination pulse, please consider the actual lighting delay in the Line cycle and illumination lighting period.